



3101S2

Triconex Tri-GP Main Processor Module

Product scope

- Executes one channel of the three-processor Tri-GP architecture.
- Uses a dedicated I/O processor for the 2 Mbit/s field-data path.
- Provides flash, DRAM, shared memory and monitored NVRAM resources.
- This ordering code identifies the Tri-GP v2 main processor fitted to the 2101S2 processor baseplate.

Official source basis

Invensys Triconex, Planning and Installation Guide for Triconex General Purpose v2 Systems, Main Processor Components.

Technical facts are limited to the identified manufacturer documentation and the exact ordering configuration shown above.

Request a fast quote	Product reference	
Email: info@apterpower.com Phone: +86 18106909650 apter.com/inquiry.php	Triconex 3101S2	

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3101S2 technical profile

Triconex 3101S2 is one of the three main processors required by a Tri-GP v2 controller. Each channel runs independently while high-speed TriBus links let the processors compare data and maintain fault-tolerant operation.

A dedicated I/O processor handles the two-megabit-per-second I/O bus, leaving the program processor to execute application logic. Local flash, DRAM, shared memory and battery-monitored NVRAM support program storage, diagnostics and retained data.

Replacement planning must preserve a three-module processor set, approved firmware, project checksum and the 2101S2 baseplate arrangement. Record Ethernet, Modbus, alarm-relay and debug connections before disturbing the controller.

Selection notice

3101S2 replacement requires a verified Tri-GP v2 firmware and application baseline; do not mix an unapproved processor revision into the three-channel set.

Technical specifications

Processors per controller	3
Processor architecture	MPC860A
Program memory	16 MB DRAM
Flash memory	6 MB
Shared memory	128 KB
Retentive memory	8 KB NVRAM
Inter-processor link	TriBus
I/O bus rate	2 Mbit/s
I/O handling	Dedicated I/O processor
Logic power inputs	Dual 24 VDC
Logic regulators	3.3 V and 5 V
Ethernet interface	RJ-45
Modbus interface	DB-9
Debug interface	RJ-12
Alarm outputs	Redundant alarm relays
Compatible baseplate	2101S2
Operating temperature	0 to 60 °C
Storage temperature	-40 to 85 °C
Humidity	5 to 95%, non-condensing
System architecture	Triple Modular Redundant

Application and integration notes

Programming	• The control application is stored in flash and executed from local processor memory. • TriStation 1131 manages the controller project, downloads and online maintenance functions. • Project checksum and retentive-variable behavior must match the validated system baseline.
Diagnostics	• TriBus and diagnostic buses allow the three processors to compare channel operation. • Battery, power, communication and alarm states are exposed through front indicators and system diagnostics. • A fault in one channel is isolated so the remaining processors can continue the configured control function.
Firmware	• Processor firmware must be approved for the installed Tri-GP v2 hardware and TriStation project. • Firmware changes are controlled maintenance events and require a saved application and rollback plan. • All three processor channels should be checked for the intended revision after service.

Request product documentation and quotation support

Send the complete label, system configuration, quantity and destination.



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