

Summary of Product Number and Corresponding Documentation for the S5-155U Programmable Controller

The following table shows the assignment of the product documentation to the individual products. The listed sections of the documentation relate to the manual S5-155U (CPU 946/947) with the order no. 6ES5 998-0UM22, release 07.

Product		Product Documentation
Order No.	Title	
6ES5 155-3UA11 6ES5 155-3UA21	Central Controller S5-155U	Instructions: (Part 3): Central Controller S5-155U/155H C79000-B8576-C380-05 (Part 7): Multiprocessor Operation in the Central Controllers S5-135U/155U C79000-B8576-C500-02 User's Guide (Part 8): Multiprocessor Communication S5-135U Programmable Controller, CPU 922 and 928 S5-155U Programmable Controller, CPU 946/947 C79000-B8576-C468-05 Installation Guide (Part 2): Programmable Controllers of the U Series C79000-B8576-C452-04
6ES5 946-3UA11 6ES5 946-3UA12 6ES5 946-3UA21 6ES5 947-3UA11 6ES5 947-3UA21	CPU 946/947	Instructions (Part 4): CPU 946/947 C79000-B8576-C532-06 Programming Guide (Part 9): S5-155U Programmable Controller, CPU 946/947 and S5-155H Programmable Controller, CPU 946R/947R C79000-B8576-C637-03 List of Operations (in the front pocket) CPU 946/947, CPU 946R/947R C79000-B8576-C111-02
6ES5 355-3UA11	355 Memory Module	Instructions (Part 5): 355 Memory Module C79000-B8576-C382-06
6ES5 923-3UC11	923 C Coordinator	Instructions (Part 6): 923 C Coordinator C79000-B8576-C349-06

Chapter 1

Technical Description

CPU 946/947 is the standard central processing unit for the S5-155U programmable controller. This chapter explains its application and design and shows how it fits into the S5-155U system structure. This chapter also includes the memory assignment of CPU 946/947 and a list of technical data.

1.1 Application

CPU 946/947 is used in the central controller of the S5-155U programmable controller. You can use the 355 memory module to extend the CPU's memory up to 896 Kbytes. This memory capacity enables it to process extensive programs.

CPU 946/947 executes all STEP 5 operations at very high speed and is equipped with floating-point arithmetic. It has an integrated 64 Kword¹ RAM with parity monitoring and a real-time clock.

The following program processing levels are available individually or in combination:

- Cyclic
- Time driven (9 different time bases)
- Interrupt driven (8 interrupts at block boundaries or 4 hardware interrupts)
The interrupt priorities can be selected. CPU 946/947 can process a user program for communication with communications processors (CPs) in the smooth "STOP" mode.

Using multiprocessing, you can also operate CPU 946/947 with an additional CPU 946/947 or with a CPU of the S5-135U.

CPU 946/947 uses the STEP 5 programming language.

For details on programming see the Programming Guide for the CPU 946/947, CPU 946R/947R in this manual.

1.2 Design

CPU 946/947 consists of two plug-in central processing units, 6ES5 946-3UA21/22/23 (CPU 946) and 6ES5 947-3UA21/22/23 (CPU 947).

¹ Kword stands for kiloword (one word equals 16 bits). One kiloword equals 1024 words (2¹⁰ words).

The electronics of CPU 946 are on two printed circuit boards. Two 64-pin male connectors on the mother board link the CPU to the S5 bus and S5 local bus for CPU 946/947 communication to the backplane housing. The front panel is 22 $\frac{2}{3}$ standard plug-in stations wide. Switches, buttons, and LEDs for operating the programmable controller and displaying modes of operation and faults are on the front panel.

The electronics of CPU 947 are on one printed circuit board. Two 64-pin male connectors link the CPU to the S5 local bus for CPU 946/947 communication. It has a 15-pin front connector that enables you to connect the CPU 946/947 to a programmer, operator panel or SINEC interface module.

1.3 System Structure

This section shows how CPU 946/947 is connected to the S5 bus and explains the structure of the CPU.

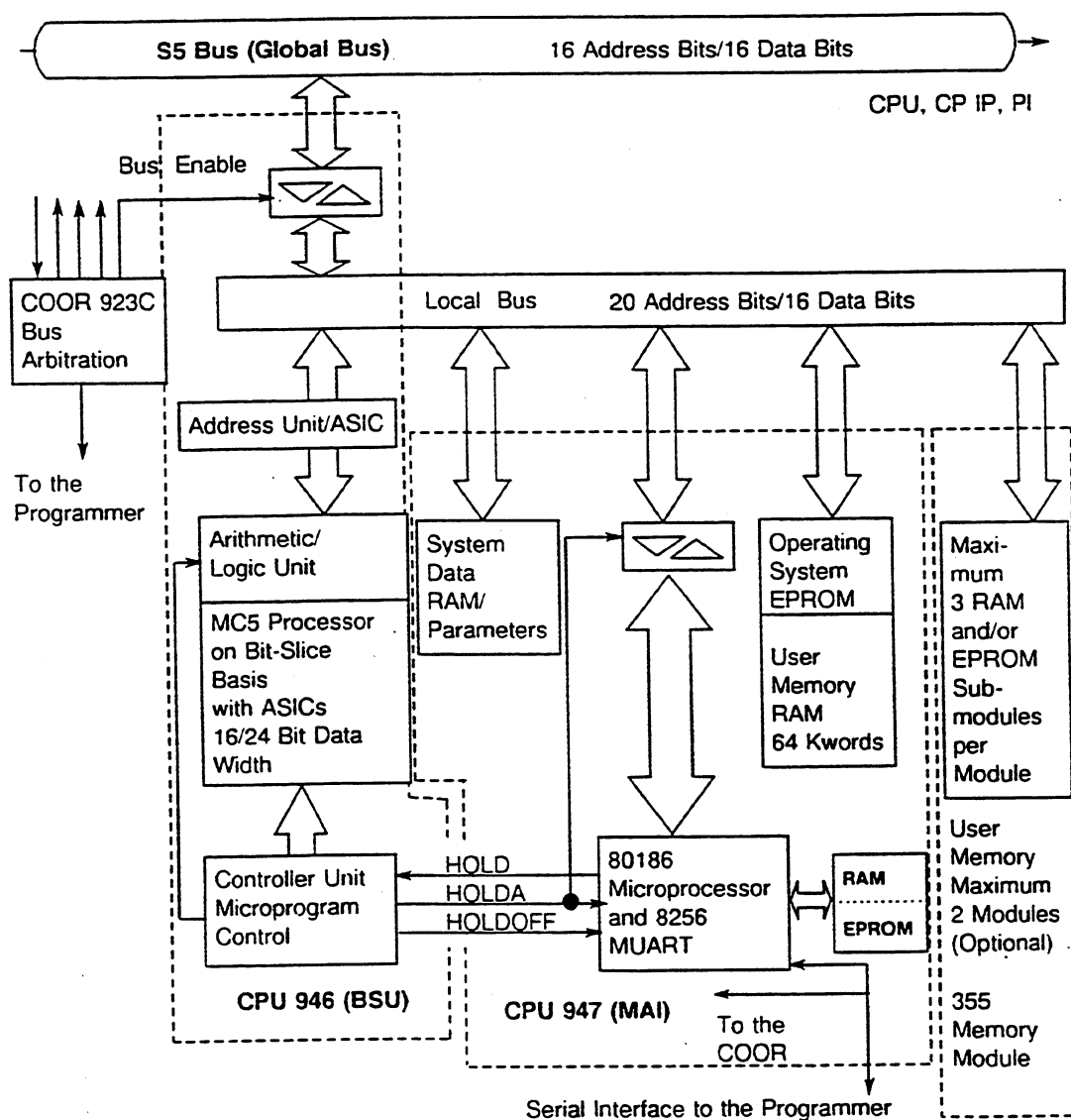


Figure 1-1 Block Diagram of CPU 946/947 with optional 355 Memory Module

The block diagram of CPU 946/947 (Fig. 1-1) shows the following two bus systems:

- **S5 bus (global bus)**
 - address bus (ADB) 16 bits wide
 - data bus (DB) 16 bits wide
- **S5 local bus**
 - local address bus (LAB) 20 bits wide
 - local data bus (LDB) 16 bits wide

The bus drivers between the S5 local bus and the S5 bus are in CPU 946. CPU 947 uses these drivers to access the S5 bus if the local bus enables have been acknowledged.

CPU 946/947 can always access the S5 bus in the single processor mode. With multiprocessing, a CPU can access the bus only through a time-slice procedure. Coordinator 923C uses time-division multiplexing to allocate bus access for each CPU.

The hardware structure of CPU 946/947 is divided into the following two large function areas:

- Bit Slice Unit (**BSU**) - in CPU 946
and
- Memory and Interface (**MAI**) - in CPU 947

CPU 946 is divided into the following three main areas:

- control unit
- arithmetic/logic unit
- address unit

CPU 947 is divided into the following two areas:

- memory unit
- communication unit

Control Unit

This unit controls the arithmetic/logic unit, the address unit, and the data flow on the buses. It reads the MC5 operations and executes them in combination with the other units. It reads all interrupts and prioritizes them.

The control unit also updates the clock and timers.

Arithmetic/Logic Unit

A special logic unit implemented as an applications-specific integrated circuit (ASIC) carries out bit operations.

An arithmetic unit (registered arithmetic/logic unit, or RALU) implemented with bit-slice components (16/24 bits) processes arithmetic and other word operations.

Address Unit

An address unit implemented as an ASIC provides addresses (20 bits). It provides optimal support for the addressing format of the STEP 5 programming language.

Memory Unit

The memory unit has a one Mword¹ memory space divided into 16 pages of 64 Kwords each. This division is not significant for the user program assignment. The pages are assigned as follows:

- Page 0 contains the 64 Kword user RAM for code and data. It is permanently integrated in CPU 947.
- Pages 1 to 6 contain RAM memory and pages 8 to D EPROM memory for user programs and user data on the optional plug-in 355 memory module with submodules.
- Page E (system page) contains a 32 Kword EPROM for the operating system. The EPROM is physically in CPU 947. The E page also contains a 31.5 Kword RAM for system data (SD RAM).
- Page F (peripherals page) contains the memory area for the peripheral units. These include inputs/outputs (I/Os), intelligent inputs/outputs (IPs), and communications processors (CPs). These units are physically on the S5 bus.

Communication Unit

An 80186 microprocessor with its accompanying memories (RAM and EPROM) is the essential component of the communication unit. The communication unit uses the serial interface in the 8256 multifunction universal asynchronous receiver transmitter (MUART) along with its internal timers and input/output ports. The 80186 microprocessor uses its own special bus-lock logic to access the S5 bus.

The communication unit can access the entire memory of CPU 946/947. You can use the interface to the programmer either directly via the front connector of CPU 947 or via the programmer multiplexer (PG-MUX).

¹ See Table 1-1

1.4 Memory Assignment

The following table shows the memory assignment for CPU 946/947. Pages 1 to 6 and 8 to D represent the user memory space in the optional 355 memory module with memory submodules.

"Page"	15	0	
0	0x2 ¹⁰	User RAM *)	0 0000 H
1	64x2 ¹⁰	User RAM	1 0000 H
2	128x2 ¹⁰	User RAM	2 0000 H
3	192x2 ¹⁰	User RAM	3 0000 H
4	256x2 ¹⁰	User RAM	4 0000 H
5	320x2 ¹⁰	User RAM	5 0000 H
6	384x2 ¹⁰	User RAM	6 0000 H
7	448x2 ¹⁰	not assigned	7 0000 H
8	512x2 ¹⁰	User EPROM	8 0000 H
9	576x2 ¹⁰	User EPROM	9 0000 H
A	640x2 ¹⁰	User EPROM	A 0000 H
B	704x2 ¹⁰	User EPROM	B 0000 H
C	768x2 ¹⁰	User EPROM	C 0000 H
D	832x2 ¹⁰	User EPROM	D 0000 H
E	896x2 ¹⁰	System Page*)	E 0000 H
F	960x2 ¹⁰	S5 Bus Peripherals Page	F 0000 H
	1024x2 ¹⁰ -1		F FFFF H

Maximum
Configuration with RAM
Submodules (No EPROM
Configuration)

Maximum Configuration with
EPROM Submodules (No
RAM Configuration)

*) Memory in CPU 947

Table 1-1 CPU 946/947 Memory Assignment

1.5 Technical Specifications

Degree of protection	IP ¹ 00		
Permissible ambient temperature			
- operation	0° C to +55° C		
- storage and transport	- 40° C to +70° C		
Relative humidity	max. 95% at 25° C, noncondensing		
Operating altitude	Up to 3500 m (11,483.5 ft.) ² above sea level		
Supply voltage	5 V DC, $\pm$ 5%		
Current consumption			
- CPU 946	approx. 6 A		
- CPU 947	approx. 2 A		
Back-up current CPU 946/947	approx. 10 μ A		
	P Area	O (Q) Area	Total
Digital inputs			
- with process image	max. 1024	-	max. 1024
- without process image	max. 1024	max. 2048	max. 3072
Analog inputs	max. 64	max. 128	max. 192
Digital outputs			
- with process image	max. 1024	-	max. 1024
- without process image	max. 1024	max. 2048	max. 3072
Analog outputs	max. 64	max. 128	max. 192
Flags	2048		
S Flags	32768		
Timers	256		
Counters	256		
Size of the user memory	64 Kwords (16 bits wide)		
Memory extension with the 6ES5 355-3UA.. and submodules	max. 384 Kwords (16 bits wide)		
Maximum memory configuration	448 Kwords (16 bits wide) (complete with RAM, or 768 Kbyte EPROM plus 128 Kbyte RAM)		
Program blocks (PB)	256		
Sequence blocks (SB)	256		
Function blocks (FB)	256		
Data blocks (DB)	256 (254 for user programs)		
Extended function blocks (FX)	256		
Extended data blocks (DX)	256 (255 for user programs)		

¹ IP stands for an environmental rating. The first number (0 to 6) after IP is the dry particle rating and the second number (0 to 8) is the moisture rating.

² Where dimensions are indicated in meters and feet, the conversion factor used is 3.281 (1 m = 3.281 ft.) with feet rounded off to the nearest tenth of a foot.

New Features and Functions from Version -3UA21, 22 onwards

The versions -3UA21 and -3UA22 are identical in their functions. For production reasons the versions were updated to 6ES5946-3UA22 and 6ES5947-3UA22.

CPU 946/947 of the S5-155U has undergone further development. The following new features have been implemented in addition to the functions of S5-DOS programmer software stage II:

- **Multiprocessing (Multi-computing)**
Operation of several similar or different complete CPUs each with their own memory and with common peripherals on the same system bus (see Chapter 10).
Integrated special functions are available for communication in multiprocessor operation (see section 10.2.2).

- Additional STEP 5 operations (see sections 3.2 through 3.4), as follows:

Basic operations:

- Load operation for double word (hexadecimal code) L DH

Supplementary operations

- Two-word substitutions DO DW, DO FW, DO =

System operations

- Add operation for double word (hexadecimal code) ADD DH
(previously ADD DF)
- Load and transfer operations for access to local and global memory areas organized in bytes or words (see Chapter 9) LY/TY GB, LW/TW GW etc.
- Load and transfer operations for access to dual-port RAM pages organized in bytes or words (see Chapter 9) LY/TY CB, LW/TW CW etc.

- New integrated special functions (see Chapter 6), as follows:

OB 124:	Delete STEP 5 blocks
OB 125:	Generate STEP 5 blocks
OB 126:	Generate process image tables
OB 200, OB 202 to OB 205:	Functions for multiprocessor communication
OB 223:	Compare CPU restart types in multiprocessor operation
OB 254, OB 255:	Transfer data blocks (DBs) and extended data blocks (DXs)

- New restart type selectable in extended data block DX 0 - retentive cold restart (see Chapter 7)
- New parameters in extended data block DX 0 for transmission of interprocessor communication (IPC) flags (see Chapter 4 and 7)
- New screen for extended data block DX0 (version 2.0 of the S5-DOS programmer software and higher). This screen offers simple parameter assignment in DX 0 (see Chapter 7).
- The STATUS online programmer function is now possible in the start-up procedure (OB 20, OB 21, OB 22) and in the smooth STOP mode (OB 39) (see section 11.6).