6.5 CPU 314C-2 PtP and CPU 314C-2 DP

Technical data

Table 6-6 Technical data of CPU 314C-2 PtP and CPU 314C-2 DP

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
CPU and version	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Order number	6ES7 314-6BF01-0AB0	6ES7 314-6CF01-0AB0
• Hardware version	01	01
• Firmware version	V2.0.0	V2.0.0
Associated programming package	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)
Memory	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
RAM		
• Integrated	48 KB	
• Expandable	No	
Load memory	Plugged in with MMC (max. 8 MB)	
Data storage life on the MMC (following final programming)	At least 10 years	
Buffering	Guaranteed by MMC (maintenance-free)	
Execution times	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Processing times of		
• Bit operations	Min. 0.1 µs	
• Word instructions	Min. 0.2 µs	
• Fixed-point arithmetic	Min. 2 µs	
• Floating-point arithmetic	Min. 6 µs	
Timers/counters and their retentivity	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
S7 counters	256	
• Retentive memory	Configurable	
• Default	from C0 to C7	
• Counting range	0 to 999	
IEC Counters	Yes	
• Type	SFB	
• Number	unlimited (limited only by RAM size)	
S7 timers	256	
• Retentive memory	Configurable	
• Default	Not retentive	
• Timer range	10 ms to 9990 s	
IEC Timers	Yes	
• Type	SFB	
• Number	unlimited (limited only by RAM size)	

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
Data areas and their retentivity	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Flag bits	256 bytes	
• Retentive memory	Configurable	
• Default retentivity	MB0 to MB15	
Clock flag bits	8 (1 byte per flag bit)	
Data blocks	Max. 511 (DB 1 to DB 511)	
• Length	max. 16 KB	
Local data per priority class	max. 510 bytes	
Blocks	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.	
OBs	See the Instruction List	
• Length	max. 16 KB	
Nesting depth		
• Per priority class	8	
• additional within an error OB	4	
FBs	Max. 512 (FB 0 to FB 511)	
• Length	max. 16 KB	
FCs	Max. 512 (FC 0 to FC 511)	
• Length	max. 16 KB	
Address areas (I/O)	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Total I/O address area	max. 1024 bytes/1024 bytes (can be freely addressed)	max. 1024 bytes/1024 bytes (can be freely addressed)
• Distributed	None	max. 1000 bytes
I/O process image	128 bytes/128 bytes	128 bytes/128 bytes
Digital channels	Max. 1016	Max. 8192
• of those local	Max. 992	Max. 992
• Integrated channels	24 DI / 16 DO	24 DI / 16 DO
Analog channels	Max. 253	Max. 512
• of those local	Max. 248	Max. 248
• Integrated channels	4 + 1 AI / 2 AO	4 + 1 AI / 2 AO
Assembly	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Racks	Max. 4	
Modules per rack	max. 8; max. 7 in rack 3	
Number of DP masters		
• Integrated	No	1
• via CP	Max. 1	Max. 1

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
Number of function modules and communication processors you can operate		
• FM	Max. 8	
• CP (PtP)	Max. 8	
• CP (LAN)	Max. 10	
Time-of-day	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Real-time clock	Yes (HW clock)	
• Buffered	Yes	
• Buffered period	Typically 6 weeks (at an ambient temperature of 40 °C)	
• Behavior of the clock on expiration of the buffered period	The clock keeps running, continuing at the time-of-day it had when power was switched off.	
• Accuracy	Deviation per day < 10 s	
Operating hours counter	1	
• Number	0	
• Value range	2^{31} hours (if SFC 101 is used)	
• Granularity	1 hour	
• Retentive	Yes; must be manually restarted after every restart	
Clock synchronization	Yes	
• In the PLC	Master	
• On MPI	Master/slave	
S7 signaling functions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Number of stations that can log in for signaling functions (e.g. OS)	Max. 12 (depends on the number of connections configured for PG / OP and S7 basic communication)	
Process diagnostics messages	Yes	
• Simultaneously enabled interrupt S blocks	Max. 40	
Testing and commissioning functions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Status/control variables	Yes	
• Variables	Inputs, outputs, memory bits, DBs, timers, counters	
• Number of variables – of those as status variable – of those as control variable	Max. 30 Max. 30 Max. 14	
Forcing	Yes	
• Variables	Inputs, outputs	
• Number of variables	Max. 10	
Block status	Yes	
Single step	Yes	
Breakpoints	2	
Diagnostic buffer	Yes	
• Number of entries (not configurable)	Max. 100	

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
Communication functions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
PG/OP communication	Yes	
Global data communication	Yes	
• Number of GD circuits	4	
• Number of GD packets – Sending stations – Receiving stations	Max. 4 Max. 4 Max. 4	
• Length of GD packets – Consistent data	max. 22 bytes 22 bytes	
S7 basic communication	Yes	
• User data per request – Consistent data	max. 76 bytes 76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)	
S7 communication		
• As server	Yes	
• as client	Yes (via CP and loadable FBs)	
• User data per request – Consistent data	max. 180 bytes (with PUT/GET) 64 bytes	
S5-compatible communication	Yes (via CP and loadable FCs)	
Number of connections	Max. 12	
can be used for		
• PG communication – Reserved (default) – Configurable	Max. 11 1 from 1 to 11	
• OP communication – Reserved (default) – Configurable	Max. 11 1 from 1 to 11	
• S7-based communication – Reserved (default) – Configurable	Max. 8 8 from 0 to 8	
Routing	No	Max. 4
Interfaces	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
1st interface		
Type of interface	Integrated RS485 interface	
Physics	RS 485	
electrically isolated	No	
Interface power supply (15 to 30 VDC)	Max. 200 mA	
Functionality		
• MPI	Yes	
• PROFIBUS DP	No	
• Point-to-point communication	No	

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
MPI		
Number of connections	12	
Services		
• PG/OP communication	Yes	
• Routing	No	Yes
• Global data communication	Yes	
• S7 basic communication	Yes	
• S7 communication – As server – As client	 Yes No (but via CP and loadable FBs)	
• Transmission rates	max. 187.5 kbps	
2nd interface	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Type of interface	Integrated RS422/RS485 interface	Integrated RS485 interface
Physics	RS 422/485	RS 485
electrically isolated	Yes	Yes
Interface power supply (15 to 30 VDC)	No	Max. 200 mA
Number of connections	None	12
Functionality		
• MPI	No	No
• PROFIBUS DP	No	Yes
• Point-to-point communication	Yes	No
DP master		
Number of connections	–	12
Services		
• PG/OP communication	–	Yes
• Routing	–	Yes
• Global data communication	–	No
• S7 basic communication	–	No
• S7 communication	–	No
• Constant bus cycle time	–	Yes
• SYNC/FREEZE	–	Yes
• Enable/disable DP slaves	–	Yes
• DPV1	–	Yes
• Transmission rates	–	Up to 12 Mbps
• Number of DP slaves per station	–	Max. 32
• Address area	–	Max. 1 KB I / 1 KB O
• User data per DP slave	–	max. 244 bytes I / 244 bytes O

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
DP slave		
Number of connections	–	12
Services		
• PG/OP communication	–	Yes
• Routing	–	Yes (only if interface is active)
• Global data communication	–	No
• S7 basic communication	–	No
• S7 communication	–	No
• Direct data exchange	–	Yes
• Transmission rates	–	Up to 12 Mbps
• Intermediate memory	–	244 bytes I / 244 bytes O
• Automatic baud rate search	–	Yes (only if interface is passive)
• Address areas		Max. 32, with max. 32 bytes each
• DPV1	–	No
GSD file	–	The latest GSD file is available at: http://www.ad.siemens.de/support in the Product Support area
Point-to-point communication		
• Transmission rates	38.4 kbps half duplex 19.2 kbps full duplex	–
• Cable length	Max. 1200 m	–
• User program can control the interface	Yes	–
• The interface can trigger a break or an interrupt in the user program	Yes (message with break ID)	–
• Protocol driver	3964 (R); ASCII and RK512	–
Programming	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Programming language	LAD/FBD/STL	
Available instructions	see the Instruction List	
Nesting levels	8	
System functions (SFCs)	see the Instruction List	
System function blocks (SFBs)	see the Instruction List	
User program security	Yes	
Integrated I/O	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
• Default addresses of the integrated – Digital inputs – Digital outputs – Analog inputs – Analog outputs	 124.0 to 126.7 124.0 to 125.7 752 to 761 752 to 755	

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
Integrated functions		
Counters	4 channels (see the Manual *Technological Functions*)	
Frequency counters	4 channels, max. 60 kHz (see the Manual *Technological Functions*)	
Pulse outputs	4 channels for pulse width modulation, max. 2.5 kHz (see the Manual *Technological Functions*)	
Controlled positioning	1 channel (see the Manual *Technological Functions*)	
Integrated "Controlling" SFB	PID controller (see the Manual *Technological Functions*)	
Dimensions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Mounting dimensions W x H x D (mm)	120 x 125 x 130	
Weight	approx. 676 g	
Voltages and currents	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Power supply (rated value)	24 VDC	
• Permitted range	20.4 V to 28.8 V	
Current consumption (no-load operation)	Typically 150 mA	
Inrush current	Typically 11 A	
Power consumption (nominal value)	800 mA	1000 mA
I^2t	0.7 A^2s	
External fusing of power supply lines (recommended)	LS switch type C min. 2 A, LS switch type B min. 4 A	
Power loss	Typically 14 W	

CPU 313C, CPU 313C-2 DP/PtP, CPU 314C-2 DP/PtP: DI/DO (connectors X11 and X12)

X11 of CPU 313C-2 PtP/DP
X12 of CPU 314C-2 PtP/DP

Standard DI	Interrupt input	Count	Posi-tioning 1)					Positioning 1) Digital	Positioning 1) Analog	Count	Standard DO
				1 ∅	1L+	2L+	∅ 21				
X	X	Z0 (A)	A 0	2 ∅	DI+0.0	DO+0.0	∅ 22			V0	X
X	X	Z0 (B)	B 0	3 ∅	DI+0.1	DO+0.1	∅ 23			V1	X
X	X	Z0 (HW gate)	N 0	4 ∅	DI+0.2	DO+0.2	∅ 24			V2	X
X	X	Z1 (A)	Prob 0	5 ∅	DI+0.3	DO+0.3	∅ 25			V3 1)	X
X	X	Z1 (B)	Bero 0	6 ∅	DI+0.4	DO+0.4	∅ 26				X
X	X	Z1 (HW gate)		7 ∅	DI+0.5	DO+0.5	∅ 27				X
X	X	Z2 (A)		8 ∅	DI+0.6	DO+0.6	∅ 28		CONV_EN		X
X	X	Z2 (B)		9 ∅	DI+0.7	DO+0.7	∅ 29		CONV_DIR		X
				10 ∅		2M	∅ 30				
				11 ∅		3L+	∅ 31				
X	X	Z2 (HW gate)		12 ∅	DI+1.0	DO+1.0	∅ 32	R+			X
X	X	Z3 (A)		13 ∅	DI+1.1	DO+1.1	∅ 33	R-			X
X	X	Z3 (B)	1)	14 ∅	DI+1.2	DO+1.2	∅ 34	Rapid			X
X	X	Z3 (HW gate)		15 ∅	DI+1.3	DO+1.3	∅ 35	Creep			X
X	X	Z0 (Latch)		16 ∅	DI+1.4	DO+1.4	∅ 36				X
X	X	Z1 (Latch)		17 ∅	DI+1.5	DO+1.5	∅ 37				X
X	X	Z2 (Latch)		18 ∅	DI+1.6	DO+1.6	∅ 38				X
X	X	Z3 (Latch)	1)	19 ∅	DI+1.7	DO+1.7	∅ 39				X
				20 ∅	1M	3M	∅ 40				

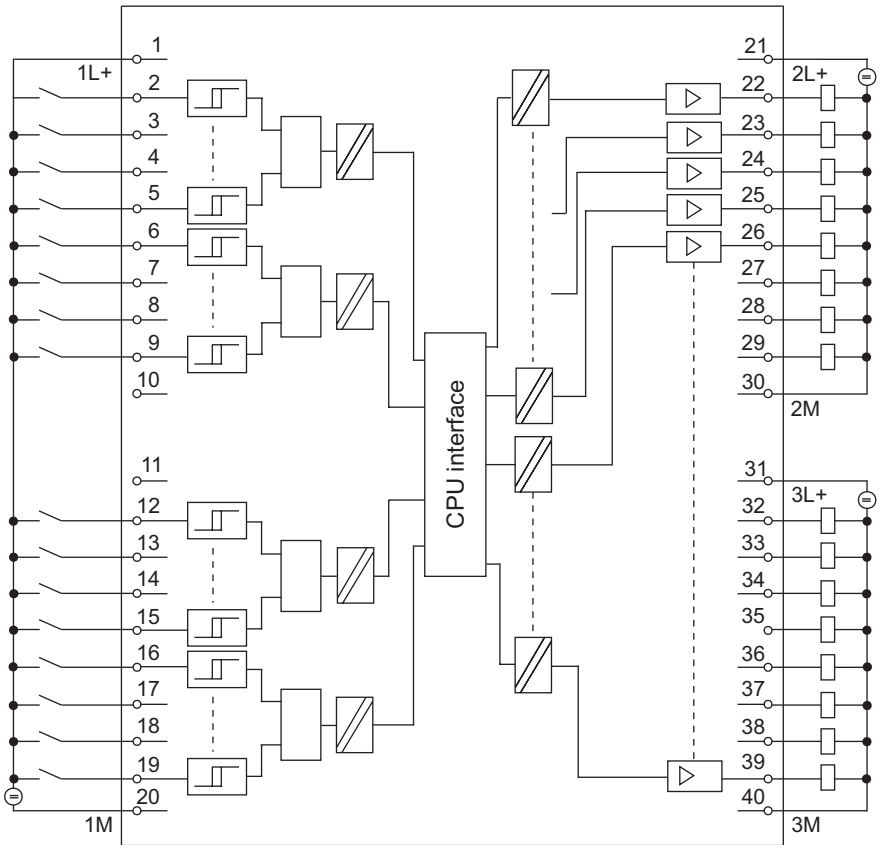
Zn	Counter n
A, B	Encoder signals
HW gate	Gate control
Latch	Store counter distance
Vn	Comparator n
Prob 0	Measuring probe 0
Bero 0	Reference point switch 0
R+, R-	Directional signal
Rapid	Rapid traverse
Creep	Creep speed
CONV_EN	Power section enable
CONV_DIR	Directional signal (only with control type "voltage 0 to 10 V or current from 0 to 10 mA and directional signal")
X	Pin usable if not assigned to technology functions

1) CPU 314C-2 only

Reference

Details are found in the Manual *Technical Functions* under *Counting, Frequency Measurement and Pulse Width Modulation*

Block diagram of integrated digital I/O of CPUs 313C/313C-2/314C-2

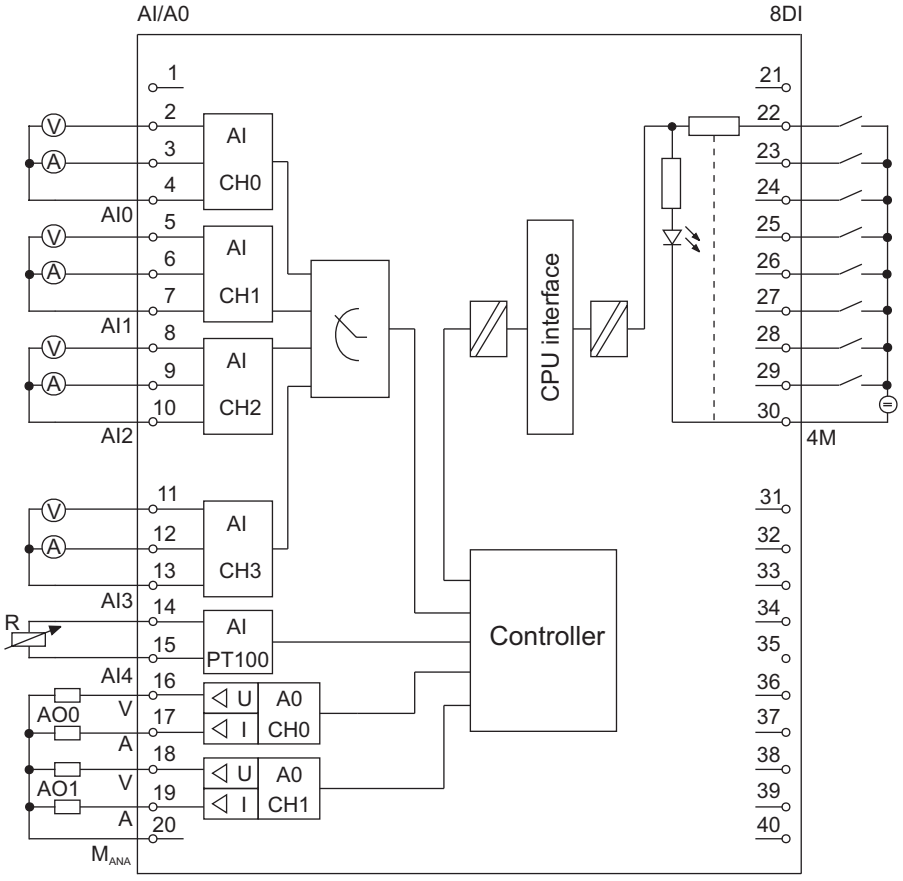


CPU 313C/314C-2: Pin-out of the integrated AI/AO and DI (connector X11)

Standard		Positioning 1)	X11				Standard DI	Interrupt input
			1 ∅			∅ 21		
AI (Ch0)	V		2 ∅	PEWx+0	DI+2.0	∅ 22	X	X
	I		3 ∅		DI+2.1	∅ 23	X	X
	C		4 ∅		DI+2.2	∅ 24	X	X
AI (Ch1)	V		5 ∅	PEWx+2	DI+2.3	∅ 25	X	X
	I		6 ∅		DI+2.4	∅ 26	X	X
	C		7 ∅		DI+2.5	∅ 27	X	X
AI (Ch2)	V		8 ∅	PEWx+4	DI+2.6	∅ 28	X	X
	I		9 ∅		DI+2.7	∅ 29	X	X
	C		10 ∅		4M	∅ 30		
AI (Ch3)	V		11 ∅	PEWx+6		∅ 31		
	I		12 ∅			∅ 32		
	C		13 ∅			∅ 33		
PT 100 (Ch4)			14 ∅	PEWx+8		∅ 34		
			15 ∅			∅ 35		
AO (Ch0)	V	Control output 0	16 ∅	PAW x+0		∅ 36		
	A		17 ∅			∅ 37		
AO (Ch1)	V		18 ∅	PAW x+2		∅ 38		
	A		19 ∅			∅ 39		
			20 ∅	M_{ANA}		∅ 40		

1) CPU 314C-2 only

Block diagram of integrated digital/analog I/O of CPUs 313C/314C-2



Simultaneous usage of technological functions and standard I/O

Technological functions and standard I/O can be used simultaneously with appropriate hardware. For example, you can use all digital inputs not used for counting functions as standard DI.

Read access to inputs used by technological functions is possible. Write access to outputs used by technological functions is not possible.

See also

CPU 312C (Page 6-3)

CPU 313C (Page 6-8)

CPU 313C-2 PtP and CPU 313C-2 DP (Page 6-14)

CPU 314C-2 PtP and CPU 314C-2 DP (Page 6-21)