

SIMATIC

Automation System S7-400 CPU Specifications

Reference Manual

Preface, Contents

Structure of a CPU 41x

Memory Concept and
Startup Scenarios

Cycle and Reaction Times
of the S7-400

Technical Specifications

Index

1

2

3

4

This manual is part of the documentation
package with the order number
6ES7398-8AA03-8BA0

Edition 12/2002

A5E00165965-01

1.13.5 Consistent Data Access without the Use of SFC 14 or SFC 15

Consistent data access of > 4 bytes without using SFC 14 or SFC 15 is possible for the CPUs listed below. The data area of a DP slave that should transfer consistently is transferred to a process image partition. The information in this area are therefore always consistent. You can subsequently use load/transfer commands (such as L EW 1) to access the process image. This is an especially convenient and efficient (low runtime load) way to access consistent data. This allows efficient integration and configuration of drives or other DP slaves, for example.

This applies to CPUs with firmware version 3.0 or later:

S7-400 CPU	MLFB
CPU 412-1	6ES7412-1XF03-0AB0
CPU 412-2	6ES7412-2XG00-0AB0
CPU 414-2	6ES7414-2XG03-0AB0
CPU 414-3	6ES7414-3XJ00-0AB0
CPU 416-2	6ES7416-2XK02-0AB0
CPU 416-3	6ES7416-3XL00-0AB0
CPU 417-4	6ES7417-4XL00-0AB0

No I/O access error occurs with direct access (e.g. L PEW or T PAW).

The following is important for converting from the SFC14/15 method to the process image method:

- When converting from the SFC14/15 method to the process image method, it is not recommended to use the system functions and the process image at the same time. Although the process image is updated when writing with the system function SFC15, this is not the case when reading. In other words, the consistency between the process image values and the values of the system function SFC14 is not ensured.
- SFC 50 "RD_LGADR" outputs another address area with the SFC 14/15 method as with the process image method.
- If you are using a CP 443-5 ext the simultaneous use of SFC 14/15 and the process image results in the following errors, you cannot read/write into the process image and/or you can no longer read/write with SFC 14/15.

Technical Specifications

4

Chapter overview

In Section	You Will Find	On Page
4.1	Technical Specifications of the CPU 412-1; (6ES7412-1XF03-0AB0)	4-2
4.2	Technical Specifications of the CPU 412-2; (6ES7412-2XG00-0AB0)	4-6
4.3	Technical Specifications of the CPU 414-2; (6ES7414-2XG03-0AB0)	4-10
4.4	Technical Specifications of the CPU 414-3; (6ES7414-3XJ00-0AB0)	4-14
4.5	Technical Specifications of the CPU 416-2; (6ES7416-2XK02-0AB0, 6ES7416-2FK02-0AB0)	4-18
4.6	Technical Specifications of the CPU 416-3; (6ES7416-3XL00-0AB0)	4-22
4.7	Technical Specifications of the CPU 417-4; (6ES7417-4XL00-0AB0)	4-26
4.8	Technical Specifications of the Memory Cards	4-30

4.7 Technical Specifications of the CPU 417-4; (6ES7417-4XL00-0AB0)

CPU and Version			
MLFB	6ES7417-4XL00-0AB0	• Size	Max. 64 Kbytes
• Firmware version	V 3.1	Local data (can be set)	Max. 64 Kbytes
Associated programming package	As of STEP7 V 5.2	• Preset	32 Kbytes
Memory		Blocks	
Working memory		OBS	See instruction list
• Integrated	2 Mbytes for code 2 Mbytes for data	• Size	Max. 64 Kbytes
• Expandable	Up to 10 Mbytes for code Up to 10 Mbytes for data	Nesting depth	
Load memory		• Per priority class	24
• Integrated	256 Kbytes RAM	• Additionally in an error OB	2
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes	FBs	Max. 6144
• Expandable RAM	With memory card (RAM) up to 64 Mbytes	• Size	Max. 64 Kbytes
Backup	Yes	FCs	Max. 6144
• With battery	All data	• Size	Max. 64 Kbytes
• Without battery	None		
Processing Times		Address Areas (Inputs/Outputs)	
Processing times for		Total I/O address area	16 Kbytes/16 Kbytes
• Bit operations	Min. 0.1 µs	• Of which distributed	
• Word instructions	Min. 0.1 µs	MPI/DP interface	2 Kbytes/2 Kbytes
• Integer math instructions	Min. 0.1 µs	DP interface	8 Kbytes/8 Kbytes
• Floating-point math instructions	Min. 0.6 µs	The distributed I/O address area is halved for each strand operated clock synchronously, i.e. in which an OB 61 to OB 64 is assigned.	
Timers/Counters and Their Retentivity		Process Image	16 Kbytes/16 Kbytes (can be set)
S7 counters	512	• Preset	1024 bytes/1024 bytes
• Retentivity can be set	From Z 0 to Z 511	• Number of partial process images	Max. 15
• Preset	From Z 0 to Z 7	• Consistent data	Max. 244 bytes
• Counting range	1 to 999	Digital channels	131072/131072
IEC counter	Yes	• Of which central	131072/131072
• Type	SFB	Analog channels	8192/8192
S7 timers	512	• Of which central	8192/8192
• Retentivity can be set	From T 0 to T 511		
• Preset	No retentive timers		
• Time range	10 ms to 9990 s		
IEC timers	Yes		
• Type	SFB		
Data Areas and Their Retentivity			
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)		
Memory markers	16 Kbytes		
• Retentivity can be set	From MB 0 to MB 16383		
• Preset retentivity	From MB 0 to MB 15		
Clock memories	8 (1 memory byte)		
Data blocks	Max. 8191 (DB 0 reserved)		