

SIMATIC

Automation System S7-400 CPU Specifications

Reference Manual

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1.13.5 Consistent Data Access without the Use of SFC 14 or SFC 15

Consistent data access of > 4 bytes without using SFC 14 or SFC 15 is possible for the CPUs listed below. The data area of a DP slave that should transfer consistently is transferred to a process image partition. The information in this area are therefore always consistent. You can subsequently use load/transfer commands (such as L EW 1) to access the process image. This is an especially convenient and efficient (low runtime load) way to access consistent data. This allows efficient integration and configuration of drives or other DP slaves, for example.

This applies to CPUs with firmware version 3.0 or later:

S7-400 CPU	MLFB
CPU 412-1	6ES7412-1XF03-0AB0
CPU 412-2	6ES7412-2XG00-0AB0
CPU 414-2	6ES7414-2XG03-0AB0
CPU 414-3	6ES7414-3XJ00-0AB0
CPU 416-2	6ES7416-2XK02-0AB0
CPU 416-3	6ES7416-3XL00-0AB0
CPU 417-4	6ES7417-4XL00-0AB0

No I/O access error occurs with direct access (e.g. L PEW or T PAW).

The following is important for converting from the SFC14/15 method to the process image method:

- When converting from the SFC14/15 method to the process image method, it is not recommended to use the system functions and the process image at the same time. Although the process image is updated when writing with the system function SFC15, this is not the case when reading. In other words, the consistency between the process image values and the values of the system function SFC14 is not ensured.
- SFC 50 "RD_LGADR" outputs another address area with the SFC 14/15 method as with the process image method.
- If you are using a CP 443-5 ext the simultaneous use of SFC 14/15 and the process image results in the following errors, you cannot read/write into the process image and/or you can no longer read/write with SFC 14/15.

Memory Concept and Startup Scenarios

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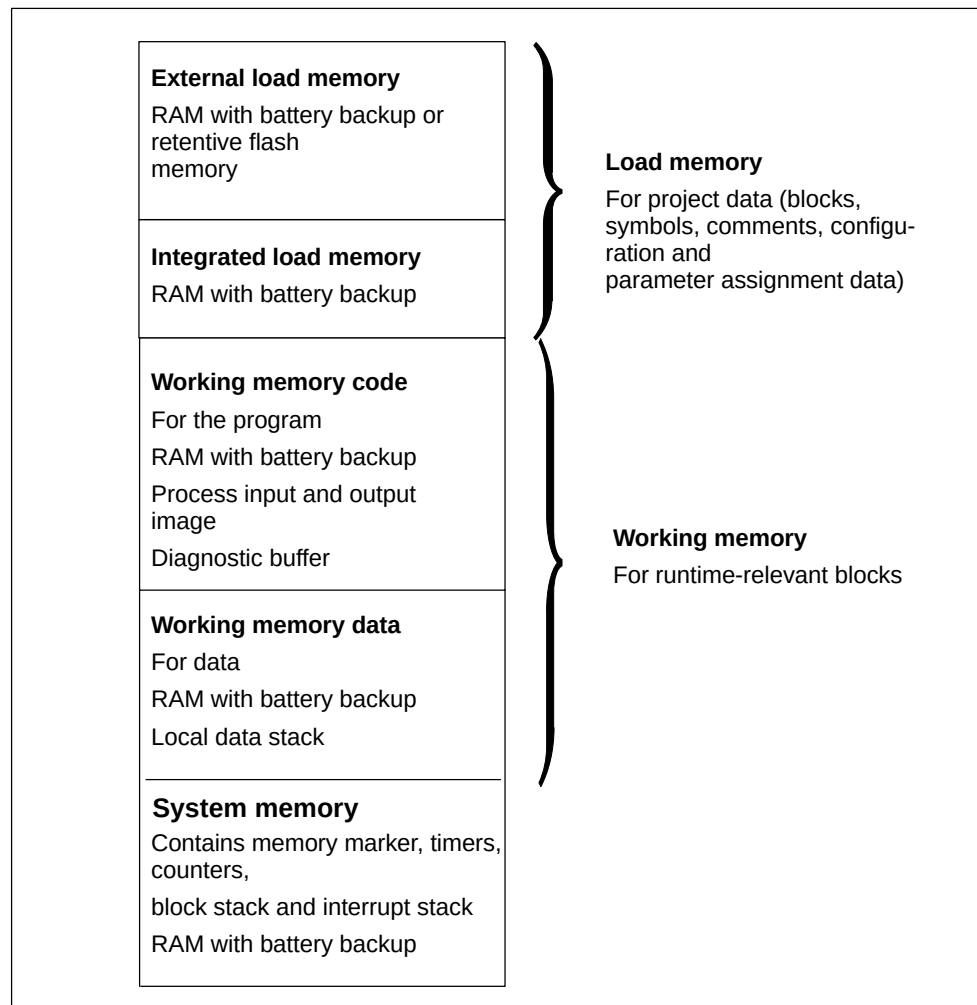
Chapter Overview

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2.1 Overview of the Memory Concept of S7-400 CPUs

Subdivision of the Memory Areas

You can divide the memory of the S7 CPUs into the following areas:



Important Note for CPUs with Configurable Division of the Working Memory

If you use parameter assignment to change the division of the working memory, the working memory is reorganized when the system data are downloaded to the CPU. The result of this is that data blocks that were created with SFC are deleted, and the remaining data blocks are assigned initial values from the load memory.

The usable size of the working memory for code or data blocks is changed if you change the following parameters for loading the system data:

- Size of the process image (byte by byte; "Cycle/Clock Memory" tab)
- Communication resources (S7-400 only; "Memory" tab)
- Size of the diagnostic buffer ("Diagnostics/Clock" tab)
- Number of local data for all priority classes ("Memory" tab)

Basis for Calculating the Required Working Memory

To ensure that you do not exceed the available amount of working memory in the CPU, you must take into consideration the following memory requirements when assigning parameters:

Table 2-1 Memory Requirements

Parameter	Required Working Memory	In Code/Data Memory
Size of the process image (inputs)	12 bytes per byte in the process input image	Code memory
Size of the process image (outputs)	12 bytes per byte in the process output image	Code memory
Communication resources (communication jobs)	72 bytes per communication job	Code memory
Size of diagnostic buffer	20 bytes per entry in the diagnostic buffer	Code memory
Volume of local data	1 byte per byte of local data	Data memory

Memory Types in S7-400 CPUs

- Load memory for project data, such as blocks, configuration and parameter assignment data, including symbols and comments as of version 5.1.
- Working memory for the runtime-relevant blocks (code blocks and data blocks).
- System memory (RAM) contains the memory elements that each CPU makes available to the user program, such as memory markers, timers, and counters. The system memory also receives the block stack and the interrupt stack.
- System memory of the CPU also makes temporary memory available (local data stack, diagnostic buffer and communication resources) that is assigned to the program when a block is called for its temporary data. These data are only valid as long as the block is active.

By changing the default values for the process image, local data, diagnostic buffer and communication resources (see the object properties of the CPU in HWCONFIG), you can control the working memory available to the runtime-relevant blocks.

Notice

Please note the following if you enlarge the process image of a CPU. Make sure that you configure the modules that can only be operated above the process image in such a way that they are also positioned above the enlarged process image. This particularly applies to IP and WF modules that you operate in the S5 adapter casing in a S7 400.

Flexible Memory Capacity

- Working memory:
The capacity of the working memory is determined by selecting the appropriate CPU from the finely graded range of CPUs.
In the case of the CPU 417, working memory can be expanded.
- Load memory:
The integrated load memory is sufficient for small and medium-sized programs.
The load memory can be increased for larger programs by inserting the RAM memory card.
Flash memory cards are also available to ensure that programs are retained in the event of a power failure even if there isn't a backup battery. Flash memory cards can also be used (as of 2 MB for standard CPUs, as of 4 MB for fault-tolerant CPUs) to send and execute operating system updates.

Backup

- The backup battery provides backup power for the integrated and external part of the load memory, the data section of the working memory and the code section.

2.2 Overview of the Startup Scenarios for S7-400-CPU's

Cold Restart

- At a cold restart, all the data (process image, memory markers, timers, counters and data blocks) are reset to the start values stored in the program (load memory) - irrespective of whether they were configured as retentive or non-retentive.
- Program processing is started from the beginning again (startup OB or OB 1).

Warm Restart

- At a warm restart, the process image and the non-retentive memory markers, timers and counters are reset.
Retentive memory markers, timers and counters and all the data blocks retain their last valid value.
- Program processing is started from the beginning again (startup OB or OB 1).
- When the power supply is interrupted, a warm restart is only possible in backed-up mode.

Restart

- At a restart, all the data, including the process image, retain their last valid value.
- Program processing is resumed at exactly the instruction at which the interruption occurred.
- The outputs are not changed until the end of the current cycle.
- When the power supply is interrupted, a restart is only possible in backed-up mode.

Technical Specifications

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Chapter overview

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4.4 Technical Specifications of the CPU 414-3; (6ES7414-3XJ00-0AB0)

CPU and Version		Data Areas and Their Retentivity	
MLFB	6ES7414-3XJ00-0AB0	Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
• Firmware version	V 3.1	Memory markers	8 Kbytes
Associated programming package	As of STEP7 V 5.2	• Retentivity can be set	From MB 0 to MB 8191
Memory		• Preset retentivity	From MB 0 to MB 15
Working memory		Clock memories	8 (1 memory byte)
• Integrated	384 Kbytes for code 384 Kbytes for data	Data blocks	Max. 4095 (DB 0 reserved)
• Expandable	No	• Size	Max. 64 Kbytes
Load memory		Local data (can be set)	Max. 16 Kbytes
• Integrated	256 Kbytes RAM	• Preset	8 Kbytes
• Expandable FEPRM	With memory card (FLASH) up to 64 Mbytes	Blocks	
• Expandable RAM	With memory card (RAM) up to 64 Mbytes	OBs	See instruction list
Backup	Yes	• Size	Max. 64 Kbytes
• With battery	All data	Nesting depth	
• Without battery	None	• Per priority class	24
Processing Times		• Additionally in an error OB	2
Processing times for		FBs	Max. 2048
• Bit operations	Min. 0.1 µs	• Size	Max. 64 Kbytes
• Word instructions	Min. 0.1 µs	FCs	Max. 2048
• Integer math instructions	Min. 0.1 µs	• Size	Max. 64 Kbytes
• Floating-point math instructions	Min. 0.6 µs	Address Areas (Inputs/Outputs)	
Timers/Counters and Their Retentivity		Total I/O address area	8 Kbytes/8 Kbytes
S7 counters	256	• Of which distributed	
• Retentivity can be set	From Z 0 to Z 255	MPI/DP interface	2 Kbytes/2 Kbytes
• Preset	From Z 0 to Z 7	DP interface	6 Kbytes/6 Kbytes
• Counting range	1 to 999	The distributed I/O address area is halved for each strand operated clock synchronously, i.e. in which an OB 61 to OB 63 is assigned.	
IEC counter	Yes	Process Image	8 Kbytes/8 Kbytes (can be set)
• Type	SFB	• Preset	256 bytes/256 bytes
S7 timers	256	• Number of partial process images	Max. 8
• Retentivity can be set	From T 0 to T 255	• Consistent data	Max. 244 bytes
• Preset	No retentive timers	Digital channels	65536/65536
• Time range	10 ms to 9990 s	• Of which central	65536/65536
IEC timers	Yes	Analog channels	4096/4096
• Type	SFB	• Of which central	4096/4096

Configuration		S7 Message Functions	
Central racks/expansion units	Max. 1/21	Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 8
Multicomputing	Max. 4 CPUs (with UR1 or UR2)	Symbol-related messages	Yes
Number of plug-in IMs (overall)	Max. 6	- Number of messages - Overall 100 ms grid 500 ms grid 1000 ms grid	Max. 512 Max. 128 Max. 256 Max. 512
- IM 460 - IM 463-2	Max. 6 Max. 4	- Number of additional values per message - With 100 ms grid - With 500, 1000 ms grid	Max. 1 Max. 10
Number of DP masters		Block-related messages	Yes
- Integrated - Via IF 964-DP - Via IM 467 - Via CP	2 1 Max. 4 Max. 10	Simultaneously active ALARM-S/SQ blocks and ALARM-D/DQ blocks	Max. 100
IM 467 cannot be used with the CP 443-5 Extended		ALARM-8 blocks	Yes
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6	Number of communication jobs for ALARM-8 blocks and blocks for S7 communication (can be set)	Max. 600
Operable function modules and communication processors		Preset	300
- FM - CP 440 - CP 441 - Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Limited by the number of slots and the number of connections Limited by the number of slots Limited by the number of connections Max. 14	Process control reports	Yes
		Number of archives that can log on simultaneously (SFB 37 AR_SEND)	16
Time		Test and Startup Functions	
Clock	Yes	Monitor/modify variable	Yes
- Buffered - Resolution - Accuracy at - Power off - Power on	Yes 1 ms Deviation per day 1.7 s Deviation per day 8.6 s	Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
Runtime meter	8	Number of variables	Max. 70
- Number - Value Range - Granularity - Retentive	0 to 7 0 to 32767 hours 1 hour Yes	Force	Yes
Time synchronization	Yes	Variables	Inputs/outputs, memory markers, distributed inputs/outputs
In PLC, on MPI, DP and IF 964 DP	as master or slave	Number of variables	Max. 256
Time of day difference in the system for synchronization via		Status block	Yes
- ETHERNET - MPI	maximum 10 ms maximum 200 ms	Single sequence	Yes
		Diagnostic buffer	Yes
		- Number of entries - Preset	Max. 3200 (can be set) 120
		Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	31 without message processing, 8 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	32, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 8
• Number of GD packages	
– Sender	Max. 8
– Receiver	Max. 16
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• User data per job	Max. 76 bytes
– Of which consistent	16 Byte
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	Yes (via CP – max. 10 – and FC AG_SEND and FC AG_RECV)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 32 DP: 16
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
MPI	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps

DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	Maximum 244 bytes E, maximum 244 bytes A, distributed over 244 slots each with 128 bytes
DP slave	
• Utilities	
– Monitor/modify	Yes, if the interface is active
– Programming	Yes, if the interface is active
– Routing	Yes, if the interface is active
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– Address areas	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes
2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	16

Functionality		System function blocks (SFB)	See instruction list
● PROFIBUS DP	DP master/DP slave	Number of SFBs active at the same time	
DP Master		● RD_REC	8
● Utilities		● WR_REC	8
– Programming device/OP communication	Yes	User program protection	Password protection
– Routing	Yes	Access to consistent data in the process image	Yes
– Equidistance	Yes	CiR synchronization time	
– SYNC/FREEZE	Yes	Base load	100 ms
– Enable/disable DP slaves	Yes	Time per I/O byte	120 μs
● Transmission rates	Up to 12 Mbps	Clock synchronism	
● Number of DP slaves	Max. 96	User data per clock synchronous slave	Max. 128 bytes
● Address area	Max. 6 Kbytes inputs/6 Kbytes outputs	Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes / 50 + number of slaves < 20
● User data per DP slave	In accordance with the DP slave, but a maximum of 128 bytes of inputs/128 bytes of outputs	Equidistance	Yes
DP slave		Shortest clock pulse	5 ms
As for the 1st interface			2.5 ms without use of SFC 126, 127
3rd Interface		Dimensions	
Type of interface	Plug-in interface submodule	Mounting dimensions W×H×D (mm)	50×290×219
Insertable interface submodule	IF-964-DP	Slots required	2
Technical features as for the 2nd interface		Weight	approx. 1.07 kg
Programming		Voltages, Currents	
Programming language	LAD, FBD, STL, SCL	Current consumption from S7-400 bus (5 VDC)	Typ. 1.5 AMax. 1.6 A
Instruction set	See instruction list	Current consumption from the S7-400 bus (24 VDC)	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Bracket levels	8	The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	
System functions (SFC)	See instruction list	Backup current	Typ 40 μA Max. 420 μA
Number of SFCs active at the same time		maximum backup time	approx 356 days
● WR_REC	8	Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
● WR_PARM	8	Power loss	Typ. 7.5 W
● PARM_MOD	1		
● WR_DPARM	2		
● DPNRM_DG	8		
● RDSYSST	1 to 8		
● DP_TOPOL	1		

CPU as DP Slave

You can only configure the CPU once as a DP slave even if the CPU has several interfaces.