

SIEMENS

SIMATIC S5

S5-155H Programmable Controller (CPU 948R / CPU 948RL)

Volume 1/2

Manual

This manual is part of the documentation package
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Part I
S5-155 H
Programmable Controller
(CPU 948R / 948RL)
Instructions

Part II
Data Handling Blocks
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Instructions

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3.1 Technical Specifications of the CPU 948R/948RL

Application

The CPU 948R and 948RL can be used in S5-135U/155H central controllers. Multiprocessor configurations are not possible in fault-tolerant systems.

The CPU 948R/948RL is available in the following versions:

CPU version	Internal user memory (RAM)
CPU 948RL	128 Kbyte
CPU 948R-1	640 Kbyte
CPU 948R-2	1664 Kbyte

A SIMATIC S5 flash EPROM memory card (referred to in the following simply as memory card) can be plugged into the CPU 948R and 948RL as storage medium for the user program and user data. On an overall reset, the contents of the memory card are copied to the CPU's internal RAM.

The CPU 948R and 948RL are programmed in STEP 5 (LAD, CSF, STL, SCL). The CPU 948R/948RL processes all STEP 5 operations at a very high speed, and is also equipped with a high-speed floating-point arithmetic facility.

The following program processing levels are possible:

- Cyclic
- Time-controlled (9 different time grids, clock-controlled, delayed interrupt)
- Interrupt-driven over the S5 bus (eight process interrupts at block boundaries via IB0)
- 'Soft STOP'

Configuration

The CPU 948R/948RL's electronics, including RAM, are on two PCBs. These PCBs have Eurocard format, and are bolted to one another. They must never be separated.

The module's frontplate has a width of 2 2/3 standard slots, or 40 mm. The CPU 948R/948RL takes up two slots in the central controller rack.

3.2 CPU 948R/948RL Installation and Startup Procedures

Note

All jumpers on the module are required for the manufacturer's quality inspection. The jumper configuration must not be changed in any way.

Removing and Inserting the Module



Caution

Always switch off the power before removing or inserting the module.

The CPU 948R/948RL's basic board and its expansion board are a unit, and must not be separated.

Inserting the module

Proceed as follows to insert the CPU in the central controller:

Step	Procedure
1	Loosen the upper locking bar on the central controller and check to make sure that the module's locking bolt is correctly positioned (that is, with the slit in the vertical position).
2	Select the right slot (check the label on the locking bar). Insert the CPU (slot 11), aligning it to the left.
3	Push the module evenly onto the guide rail until the lever above the locking bolt is in a vertical position.
4	Press in the locking bolt on the underside of the module and turn it 90° to the right.
5	Affix the upper locking bar.

Removing the module

Proceed as follows to remove the CPU:

Step	Procedure
1	Loosen the upper locking bar on the central controller.
2	Loosen the module's locking bolt.
3	Press down on the lever and remove the module by pulling it forward and out of the controller.

Control Elements and LEDs

The control elements and LEDs are arranged in the same way on the frontplate of the CPU 948R and CPU 948RL. Figure 3-1 shows an example of the frontplate of the CPU 948R.

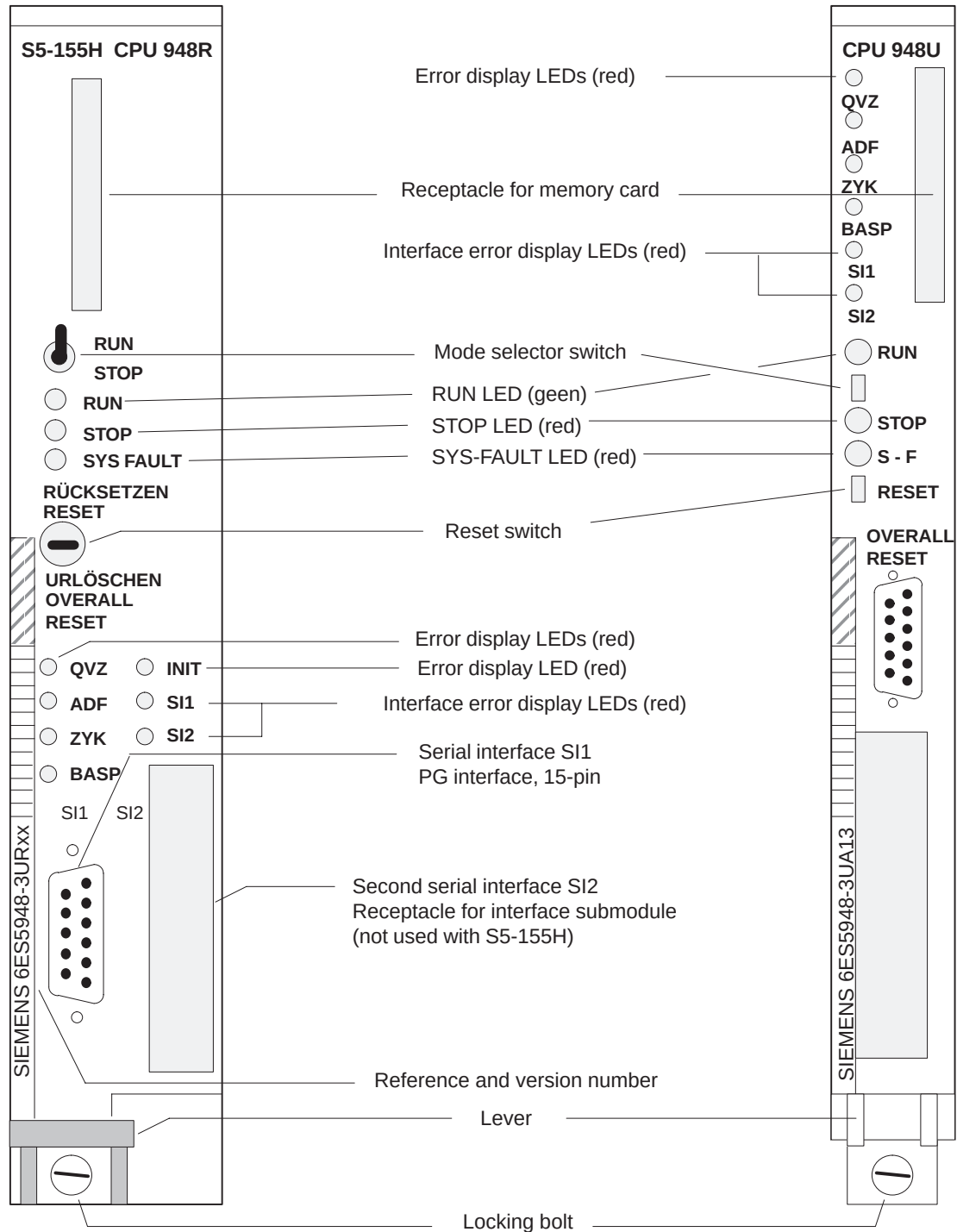


Figure 3-1 CPU 948R/948RL and CPU 948U Control Elements and LEDs

Mode Selector Switch

The mode selector switch has two positions:

- RUN

When the mode selector switch is set to 'RUN' and the green LED is on, the CPU 948R/948RL is processing the user program.

- STOP

The CPU 948R/948RL goes to 'soft STOP' when the user switches from 'RUN' to 'STOP'. The red "STOP" LED goes on.

Reset Switch

The restart functions "Overall reset", "Cold restart" and "Cold restart with memory" can be initiated via the mode selector switch and the reset switch:

Function	Switch position	Description
Overall reset (OVERALL RESET)	Down	An overall reset reinitializes the internal RAM (meaning any data currently in RAM are erased and the contents of the memory card, if any, are copied to internal RAM). A complete self-test is then executed.
Cold restart (RESET)	Up	A cold restart, or RESET, resets all flags, timers, counters and the process image. OB 20 is then called, and user program processing begins again.
Cold restart with memory	Middle	User program processing begins again, but all flags, timers, counters and the process image retain their current states.

Status LEDs

The following overview describes the LEDs for "RUN", "STOP" and "SYS FAULT".

The "STOP" LED signals a 'soft STOP', the "SYS FAULT" LED a 'hard STOP'.

In 'soft STOP' mode, the CPU 948R/948RL can scan the user program (OB 39) cyclically, but the digital outputs remain disabled. In 'hard STOP' mode, no program can run; the CPU is at a 'standstill'. This state can be exited only by switching the power off and then on again.

LED			
RUN	STOP	SYS-FAULT	Mode
RUN or RESTART mode			
On	Off	Off	The CPU is in RUN mode and is master (cyclic operation).
Flashes	Off	Off	The CPU is in RUN mode and is the standby (cyclic operation).
On	Flashes	Off	The CPU is master; the parallel link has failed.
On	On	On	Appears briefly when the controller is switched on.
On	On	Off	The CPU executes the self-test on startup.
Off	Off	Off	The CPU is in the RESTART mode or PROGRAM TEST.
'Soft STOP' mode			
Off	On	Off	The CPU is in 'soft STOP' mode. After switching on the power when the mode selector switch is at STOP and no errors occurred during initialization. A restart is possible.
Off	Flashes at high frequency	Off	The CPU is in 'soft STOP' mode. An overall reset was requested via mode selector switch/reset switch or by the operating system. A restart is possible only after performing an overall reset or after eliminating the problem and then performing an overall reset.
Off	Flashes at low frequency	Off	The CPU is in 'soft STOP' mode. - An error was detected during cyclic program processing. The CPU is at STOP because no appropriate error handling routine was programmed. When you move the mode selector switch from RUN to STOP, the LED will once again show a steady light as long as the error does not re-occur. - When error conditions exist, for example, selection of an illegal Restart mode, DB1/DX0 errors, and so on. - When a STOP operation (STP or STS) was encountered in the user program. - In the event of a PROGRAM TEST programmer function for this CPU. - Some programming errors and controller faults also set the 'ADF', 'QVZ' or 'ZYK' LEDs.
'Hard STOP' mode			
Off	Off	On	The CPU is in 'hard STOP' mode. - When error-free execution of the system program is no longer possible, the CPU enters the 'hard STOP' mode. - Reasons for a 'hard STOP': - Timeout (QVZ) or parity error (PARE) in system RAM - ISTACK overflow - STEP 5 operation "STW" - A 'hard STOP' can be exited only by turning off the controller and switching it on again.
'Activate standby' mode			
Flashes	Flashes	Off	The CPU is the standby, and the mode is 'Activate standby'.

Error LEDs

The following overview shows why and when each error LED goes on:

LED	Description
QVZ (timeout)	A module addressed by the program no longer acknowledges, although/because: - it either acknowledged in the process image (IB 0 to 127, QB 0 to 127) on a CPU 948R/948RL cold restart and was entered as available in the so-called '9th track' - or was entered in DB 1 (address list) and was recognized as being available on a cold restart - or was addressed in direct access mode - or no access is possible to the data handling blocks on the module. Possible causes: - Module failure; failure of the expansion unit - Module was removed during operation, while the CPU was at STOP or when the controller was switched off and there was no subsequent cold restart. - Failure of the enable voltage L+ A timeout occurred while user memory was being accessed.
ADF On	The user program referenced an address in the process image which was not entered in DX 1.
ZYK On	The watchdog timer used for scan time monitoring responded and cyclic program processing was interrupted.
BASP On	Command output is disabled; the digital outputs are set directly to the safe state (0).
INIT On	Applies to CPU 948 UR 11/12, 21/22 and 51: This LED briefly shows a steady light during the initialization procedure which follows POWER ON, and during operation in the event of a system fault. Applies to CPU 948 R UR 13, 23, 53: INIT LED does not exist on the front plate.

A detailed description of interrupt servicing and error handling procedures can be found in the Programming Guide for the CPU 948R (Volume 2 of this manual).

Interface Error LEDs SI1 and SI2

Reasons why the interface error LEDs go on:
LED SI2 is always off unless there is a CPU fault.

LED SI1	Reason
On	No communication possible; internal error.
Off	Both interfaces are initialized and ready.

Startup

The CPU must be inserted into the correct slot in the central controller. The backup battery must be inserted and in good working order before the CPU can be put into operation.

Overall Reset

Proceed as follows:

Step	Entry/Activity	Result
1.	Set the mode selector switch to 'STOP'.	
2.	Switch on the mains power.	The following LEDs on the CPU must go on: • Red "STOP" LED (flashes at high frequency) • Red "INIT" LED (briefly) • Red "BASP" LED
3.	Hold the reset switch in the 'OVER-ALL RESET' position and move the mode selector switch from 'STOP' to 'RUN'.	The red "STOP" LED and the RUN LED now show a steady light.

The red 'SYS FAULT' LED also goes on only if an error occurred during the overall reset. In this case, repeat the measures described. If necessary, switch the power off and then on again. If the LED is still on, the CPU module is defective.

Cold Restart

Continue as follows:

Step	Entry/Activity	Result for master
4.	Set the mode selector switch to 'STOP'.	
5.	Hold the reset switch in the RESET position and move the mode selector switch from 'STOP' to 'RUN'.	1. The red 'STOP' LED goes out 2. The red 'STOP' LED and the green 'RUN' LED go on 3. The green 'RUN' LED goes on 4. The red 'BASP' LED goes out The CPU is not in 'RUN' mode, but is still without a user program.

Cold Restart with Memory Function

The reset switch allows you to execute a manual cold restart (RESET) with memory. Please refer to the Programming Guide for the CPU 948R (Volume 2 of this manual) to see when a manual cold restart (RESET) with memory is permissible.

Step	Entry/Activity	Result for master
1.	Move the mode selector switch from 'STOP' to 'RUN'.	1. The red 'STOP' LED goes out 2. The red 'STOP' LED and the green 'RUN' LED go on 3. The green 'RUN' LED goes on 4. The red 'BASP' LED goes out

For maintenance purposes or in the event of an error, the above-mentioned startup procedures, without a user program, can be used to see whether the CPU is functioning properly.

**CPU 948R/948RL
Interfaces**

This chapter provides information on CPU 948R/948RL interfaces (ports) which can be used to connect a programmer or personal computer.

- **Programmer port SI1**

You can connect a programmer to this frontplate port regardless of the CPU's current mode.

- **Interfacing with SINEC H1 over the parallel wiring backplane**

Connecting a programmable controller with a programmer via SINEC H1 enables very-high-performance communications between the two. For example, the loading of application software into the CPU while in STOP mode is up to eight times faster than it would be if a serial port were used.

In addition to a CPU 948R/948RL, you also need a CP 143 (revision level 3), a PG 7xx programmer with SINEC H1 interface, and the STEP 5 "Single Tasking" (version 6.3 or newer) or "Multi-Tasking" (version 6.0 or newer) software.

Note

You cannot interface a subunit to SINEC H1 and still use the serial port.

Interfacing to SINEC H1 is discussed in detail in the Programming Guide for the CPU 948R.

Specifications

Important for use in the USA and Canada

The following approval certifications have been granted:



UL Listing Mark
Underwriters Laboratories (UL) to
Standard UL 508, Report E 85972



CSA Certification Mark
Canadian Standard Association (CSA) to
Standard C 22.2 No. 142, Report LR 63533

3.3 Technical Specifications

Common Technical Specifications

The following table contains the common technical specifications for the CPUs 948R and 948RL.

Characteristic/Function	Value				
Degree of protection	IP 00				
Ambient conditions Ambient temperature during operation Temperature change during operation during transport and while in storage Relative humidity Pollutant emissions: SO ₂ H ₂ S Oscillation during operation	0 to 55 °C Max. 10 K/h Max. 20 K/h Max. 95 % at 25 °C, no condensation 10 cm ³ /m ³ , 4 days 1 cm ³ /m ³ , 4 days 10 ...58 Hz (const. amplitude 0.075 mm) 58 ...500 Hz (const. acceleration 1 g)				
Noise immunity,electromagnetic compatibility (EMC) Interference suppression Limit class Conducted interference on AC supply lines Immunity against static discharge to IEC 801-2 (ESD) Immunity against high-frequency radiation	See Technical Specifications for the S5-135U/155U A (to VDE 0871) 2 kV (to IEC 801-4 (Burst) 1 kV (to IEC 801-5) Line to line 2 kV (to IEC 801-5) Line to ground Proper installation ensures an interference immunity of 4 kV contact discharge (8 kV atmospheric discharge). HF current-sourcing to IEC 801-6 Limit class 3 (up to 200 MHz), corresponding to 3 V/m				
Auxiliary power: Supply voltage Power consumption at 5 V	948R UR11, 12, 21, 22, 51: 5 V ± 5 % 3.6 A typ.		948R UR13, 23, 53: 5 V ± 5 % 0.5 A typ.		
Backup voltage: Backup current:	3.4 V 10 µA (at 25 °C) typ.				
	P area	O area	IM3 area	IM4 area	Total
Digital inputs with process image	max 1024	–	–	–	max. 1024
Digital inputs without process image	max. 1024	max. 2048	max. 2048	max. 2048	max 7168
or analog inputs	max. 64	max. 128	max. 128	max. 128	max. 448
Digital outputs with process image	max 1024	–	–	–	max. 1024
Digital outputs without process image	max. 1024	max. 2048	max. 2048	max. 2048	max 7168
or analog outputs	max. 64	max. 128	max. 128	max. 128	max. 448
Flags	2048				
S flags	32768				
Timers	256				
Counters	256				

Characteristic/Function	Value	
Baud rate of the serial programmer port	9600 bps	
Number of blocks		
Program blocks (PBs)	256	
Sequence blocks (SBs)	256	
Function blocks (FBs)	256	
Function blocks FXs)	256	
Data blocks (DBs)	256, 253 of which are programmable	
Data blocks (DXs)	256, 253 of which are programmable	
Organization blocks (OBs)	OB 1 to 39 (interfaces to the operating system)	
Integral special-function organization blocks (OBs)	OB 121, 122, 124, 125, 131 to 133, 141 to 143, 150, 151, 153, 254, 255	
Integral serial PG port	9600 bps	
Dimensions (W x H x D)	40.6 mm x 233.4 mm x 160 mm	
Weight	948R UR11, 12, 21, 22, 51: Approx. 1 kg	948R UR13, 23, 53: Approx. 0.6 kg

Differences between CPU 948R and CPU 948RL

The following table shows an overview of the differences in performance of the CPU 948R and the CPU 948RL.

Characteristic	CPU 948R	CPU 948RL
User memory size	640 Kbytes (CPU 948R-1) 1664 Kbytes (CPU 948R-2)	128 Kbytes
Execution times	See Pocket Guide 6ES5 997-3UR21	See CPU 948R
Basic scan cycle time	approx. 5 ms	approx. 15 ms
Digital inputs	Supports following I/O types: Types 1, 2, 3 and 4	Supports following I/O types: Types 1, 2 and 3
	max. 1024 inputs with process image Types 1, 2, 3 and 4 (1-, 2- or 3-channel)	max. 1024 inputs with process image Types 1, 2 and 3 (1- or 2-channel)
	+ 3072 without process image (Types 1 and 2)	+ 1024 without process image (Types 1 and 2) + 2048 without process image (Type 2)
	+ 4096 without process image with direct memory access Type 2 (1-channel switched)	+ 4096 without process image with direct memory access Type 2 (1-channel switched)
	+ direct access via page addressing (1-channel switched)	+ direct access via page addressing (1-channel switched)

Characteristic	CPU 948R	CPU 948RL
Digital outputs	Supports following I/O types: Types 8, 9, 10 and 11	Supports following I/O types: Types 8, 9, 10 and 11
	max. 1024 outputs with process image Types 8, 9, 10 and 11 (1- or 2-channel)	max. 1024 outputs with process image Types 8, 9, 10 and 11 (1- or 2-channel)
	+ 3072 without process image (Types 8 and 9, 1-channel)	+ 1024 without process image (Types 8 and 9, 1-channel) + 2048 without process image (Type 9, 1-channel)
	+ direct access via page addressing (1-channel switched)	+ direct access via page addressing (1-channel switched)
Analog inputs	Supports following I/O types: Types 13, 14, 15 and 16	Supports following I/O types: Types 13, 14 and 15
	max. 192 inputs (1-, 2- or 3-channel)	max. 64 inputs (only 1- or 2-channel)
	max. 448 inputs (1-channel switched)	max. 448 inputs (1-channel switched)
	+ direct access via page addressing (1-channel switched)	+ direct access via page addressing (1-channel switched)
Analog outputs	Supports following I/O types: Types 18, 19, 20 and 21	Supports following I/O types: Types 18, 19, 20 and 21
	max. 192 outputs (1- or 2-channel)	max. 64 outputs (1- or 2-channel)
	max. 448 outputs (1-channel switched)	max. 448 outputs (1-channel switched)
	+ direct access via page addressing (1-channel switched)	+ direct access via page addressing (1-channel switched)
CP/IP	Supports following I/O types: Types 24 and 25	Supports following I/O types: Types 24 and 25

You will find explanations on the individual I/O types in Section 4.1

Connector Pin Assignments

Please refer to Chapter 10 of the S5-135U/155U System Manual for a list of connector pin assignments on the CPU 948R/948RL's backplane connectors and front connector (programmer port). The pinout is the same as for the CPU 948.