

Spare part SIMATIC S5, CPU 948 Central
processing unit for S5-155U, 640 KB RAM

Further information

Information- and Downloadcenter (Catalogs, Brochures,...)

<http://www.siemens.de/industrial-controls/catalogs>

Industry Mall (Online ordering system)

<https://mall.industry.siemens.com>

5.2 CPU 948

This section contains the hardware description and the technical specifications of the CPU 948.

Details on programming the CPU 948 can be found in the CPU 948 Programming Guide.

5.2.1 Technical Description

This section contains information on the application, design and structure of the CPU 948.

Application

You can use the CPU 948 in single and multiprocessor operation in the S5-135U/155U central controller (see Chapter 6).

There are two versions of CPU 948:

- The CPU 948-1 offers 640 Kbytes of internal user memory (RAM).
- The CPU 948-2 offers 1664 Kbytes of internal user memory (RAM).

A SIMATIC S5 flash EPROM memory card (known as a memory card for short in the following) can be inserted in the CPU 948 as the storage medium for user program and user data. The contents of the memory card are copied into the internal RAM of the CPU upon overall reset.

The programming language is STEP 5 (LAD, CSF, STL, SCL). The CPU 948 processes all STEP 5 operations at very high speed, and uses fast floating-point arithmetic.

The following program processing levels are possible:

- Cyclic
- Time-controlled (9 different timebases, real-time controlled, timeout)
- Interrupt-driven from the S5 bus (8 process interrupts at block boundaries via IB0 or, alternatively, 4 system interrupts)
- Soft STOP.

Design

The electronic circuitry of the CPU 948, including the RAM, is on two PCBs of double Eurocard format which are screwed to each other. The two PCBs must not be separated. The front plate width of the module is 2 2/3 standard plug-in stations, i.e. 40 mm. In the central controller rack, the CPU 948 occupies two slots.

Startup

The modules must be inserted at the correct slots in the central controller.
The backup battery must be fitted and in order for the CPU to start.

Overall Reset

Proceed as follows:

Step	Action	Resultat
1	Set the mode switch to STOP.	
2	Switch the system voltage on.	The following LEDs must light up on the CPU: – Red STOP LED (flashing rapidly) – Red INIT LED, briefly – Red BASP ²⁾ LED
3	Hold the MC ¹⁾ switch in the OVERALL RESET setting and simultaneously set the mode switch from STOP to RUN.	The red STOP LED is now permanently lit.

1) MC: Momentary-contact

2) BASP: Command output inhibit

If the red SYS FAULT LED also lights up, an error has occurred during overall reset. In this case the measures described must be repeated. If necessary, switch the system voltage off and on again.
If the LED is still lit, the module is faulty.

Reset

Continue as follows:

Step	Action	Result
4	Set the mode switch to STOP.	
5	Hold the MC switch in the RESET setting and simultaneously set the mode switch from STOP to RUN.	– Red STOP LED goes off – Green RUN LED lights up – Red BASP LED goes off The CPU is now in the RUN state but still has no user program.

5.2.3 Interfaces of the CPU 948

This section contains information on the interfaces of the CPU 948.

PG Interface SI1

You can use the PG interface on the CPU 948 either via the front connector or via the 923C coordinator module and the S5 bus.

Note

Simultaneous operation of the PG interface via the front connector of the CPU 948 and via the 923C coordinator is not possible. Switching the PG online without a job request is already sufficient to operate the interface. Electrically, it is merely a PG interface which can be operated via two different terminals.

The connection to the PG can be established in every operational state of the CPU.

Interface SI2

You can also use the second interface of the CPU 948 as a PG interface. Physical adaptation is achieved with a PG module (see also Section 5.9, Interface Submodules).

A detailed description of PG interfaces can be found in the CPU 948 Programming Guide.

Communication via Parallel Backplane Bus with SINEC H1

A PG-PLC link via SINEC H1 allows very advanced communication between the partners. For example, the user software can be loaded into the CPU 948 up to eight-times faster than with serial communication.

For this link you will need, in addition to the CPU 948, a CPU 143 (Version ≥ 2.1) in the PLC and a PG7xx with SINEC H1 connection and the STEP 5 single-tasking software from Version 6.0 or multi-tasking from Version 2.0.

Note

You cannot implement communication via SINEC H1 in parallel with the serial interfaces.

Communication via SINEC H1 is described in detail in the CPU 948 Programming Guide.

5.2.4 Technical Specifications

Important for the USA and Canada

The following approvals have been obtained:

- UL Listing Mark
Underwriters Laboratories (UL) to Standard UL 508, Report E 85972
- CSA Certification Mark
Canadian Standard Association (CSA) to Standard C 22.2 No. 142, Report LR 63533

Degree of protection	IP 00				
Climatic ambient conditions	See Technical Specifications of the S5-135U/155U CC				
Mechanical ambient conditions	See Technical Specifications of the S5-135U/155U CC				
Noise immunity, electromagnetic compatibility (EMC)	See Technical Specifications of the S5-135U/155U CC				
Supply voltage	5 V $\pm$ 5 %				
Current consumption at 5 V	3.6 A typical				
Backup voltage	3.4 V				
Backup current	10 μ A typical (at 25 °C)				
	P area	O area	IM3 area	IM4 area	Total
Digital inputs with process image	1024 max.	–	–	–	1024 max.
Digital inputs without process image or analog inputs	1024 max. 64 max.	2048 max. 128 max.	2048 max. 128 max.	2048 max. 128 max.	7168 max. 448 max.
Digital outputs with process image	1024 max.	–	–	–	1024 max.
Digital outputs without process image or analog outputs	1024 max. 64 max.	2048 max. 128 max.	2048 max. 128 max.	2048 max. 128 max.	7168 max. 448 max.
Flags	2048				
S flags	32768				
Timers	256				
Counters	256				
Size of user memory	640 or 1664 Kbyte RAM				
Transmission rate of serial PG interface	9600 bps				
Program blocks PB	256				
Sequence blocks SB	256				
Function blocks FB	256				
Function blocks FX	256				

Data blocks DB	256, of which 253 are freely available
Data blocks DX	256, of which 253 are freely available
Organization blocks OB	OB 1 to 39 (interfaces for operating system)
Integrated special function organization blocks OB	OB 121, 122, 124-126, 131-133, 141-143, 150, 151, 153, 200, 202-205, 222, 223, 254, 255
Integrated serial interface	PG interface
Optional serial interface	PG interface with PG submodule
Backplane bus	S5 bus
Dimensions (w x h x d)	40.6 x 233.4 x 160 mm
Weight	Approx. 1 kg

For Chapter 5

CPUs	
CPU 948-1 (640 Kbyte user memory)	6ES5 948-3UA13
CPU 948-2 (1664 Kbyte user memory)	6ES5 948-3UA23
CPU 928B	6ES5 928-3UB21
CPU 928	6ES5 928-3UA21
CPU 922	6ES5 922-3UA11
374 Memory Cards	
256 Bbytes	6ES5 374-2FH21
512 Bbytes	6ES5 374-2FJ21
1028 Bbytes	6ES5 374-2FK21
2048 Bbytes	6ES5 374-2FL21
4112 Bbytes	6ES5 374-2FM21
376 Memory Cards	
16 Bbytes	6ES5 376-0AA11
32 Bbytes	6ES5 376-0AA21
64 Bbytes	6ES5 376-0AA31
377 Memory Cards	
16 Bbytes	6ES5 377-0AA11
32 Bbytes	6ES5 377-0AA21
64 Bbytes	6ES5 377-0AA32
64 Kbytes (with backup battery)	6ES5 377-0BA31
Backup battery	6ES5 980-0DA11
Interface Submodules	
PG submodule	6ES5 752-0AA53
TTY submodule for 20 mA current loop	6ES5 752-0AA12
V.24 (RS-232C) submodule	6ES5 752-0AA22
RS422-A/485 submodule	6ES5 752-0AA42
SINEC L1 submodule	6ES5 752-0AA62
Cover for submodule receptacle	C79458-L957-B51
BT 777 bus terminal	6ES5 777-xxx00
Standard connecting cables	
CPU 948/928B - PG 7xx	6ES5 734-2xxx0
CPU 928B - CP 544/525/524	
(RS422-A/485)	6ES5 725-7xxx0
CPU 928B - CP 544/525/524 (TTY)	6ES5 726-1xxx0
CPU 928B - CP 544/525/524 (V.24)	6ES5 726-8xxx0
CPU 928B - DR 210/DR 211	
DR 230/DR 231	
(TTY/V.24)	6ES5 726-5xxx0
(xxx = SIMATIC length code, see Catalog)	