System Description

ABB Procontic T300

Functional Description PLC
35 ZE 94
Version 8

Order No.: GATS 1315 11 R2001

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10 Communication with I/O modules and preprocessors

The ABB Procontic T300 system provides an extensive range of I/O modules and preprocessors with which the PLC can communicate.

10.1 Communication with I/O modules

The PLC processes the I/O signals via the process diagram, i.e. it does not access the assigned I/O modules during the program function.

Input signals

Before each program cycle, all input signals (operand identifiers E and EW) occurring in the program are written into the operand memory as an image.
This implies the advantage that consistent values of the input signals (actual values) can be used during the processing.

Output signals

During the program cycle, all output signals (operand identifiers A and AW) occurring in the program are written into a program-specific output image in the operand memory. The PLC outputs the output image at the the end of each program cycle. In multi-processor mode, *several* PLC processors must *not* write to the *same* binary output group because the different PLCs will otherwise mutually overwrite each others' output values on the output device (see also chapter entitled "Multi-processor operation"). Different programs of *one* PLC, however, may write to one binary output group. In this case, mutual overwriting is prevented by the PLC's operating system.
The above statements also apply to superglobal values.

Marshalling

All I/O operands are assigned to physical addresses (module addresses) by way of a marshalling list. In conformity with DIN 66264, this marshalling list is called the data block directory (DBV). Each PLC possesses a default data block directory which, if required, can be reconfigured very easily by the user (see also Chapter "Data block directory").

Enabling the I/Os

All I/O operands occurring in the user program are enabled for input or output by means of the PA command. I/O operands which are not planned in the user program are *ignored* by the PLC during input and output. As from PLC version V 6.0, the PA command is executed automatically with each program start.

I/O test mode

In this mode of operation, only the I/O signals are processed and the user program is not executed (see also "Operating and test functions").

Alarm inputs

The 35 EB 92 binary input module has 8 alarm inputs which may trigger a group alarm in the station which supplies the MPST bus clock. If this is a PLC, every alarm causes an event-controlled PLC program to run through precisely one program cycle. In this PLC program, the inputs occurring in it are then read in and can be evaluated.

Alarm vector

When an alarm is issued, the input module sends an alarm vector to the PLC. This alarm vector's value is set on the input module by means of the DIL switch S3.

Either program 1 or 2 is run in the PLC supplying the bus clock depending on the alarm vector's value.

Alarm vector	Reaction of the PLC
0...7 ($0...7_H$)	forbidden on 35 EB 92; this vector is allocated to the 35 IV 90 iconic image processor
8...23 ($8_H...17_H$)	Execution of a program cycle in PLC program 2
24...39 ($18_H...27_H$)	Execution of a program cycle in PLC program 1

After reception of the alarm vector by the PLC, it takes around 0.85 ms before a new cycle begins in the allocated cycle.

10.2 Default jumpering of the I/O signals and I/O modules

The data block directory (DBV) defines the I/O operands' assignments to the physical addresses. If required, the user can easily modify these assignments, but this is only necessary in rare cases.

With the default jumpering, physical addresses are:

- Addresses of I/O modules
- Addresses of global value memories
- Addresses of the super global value memory

Each I/O module address must be set on a DIL switch.

The following default marshalling applies if the user does not alter the data block directory:

Binary inputs

E 00,00...E 00,15 is jumpered to module address $E000_H$
E 01,00...E 01,15 is jumpered to module address $E002_H$
.
.
E 63,00...E 63,15 is jumpered to module address $E07E_H$

Word inputs

EW 00,00 is jumpered to module address $E100_H$
EW 00,01 is jumpered to module address $E102_H$
.
.
EW 13,15 is jumpered to module address $E2BE_H$

Binary outputs

A 00,00...A 00,15 is jumpered to module address $E080_H$
A 01,00...A 01,15 is jumpered to module address $E082_H$
.
.
A 63,00...A 63,15 is jumpered to module address $E0FE_H$

Word outputs

AW 00,00 is jumpered to module address $E300_H$
AW 00,01 is jumpered to module address $E302_H$
.
.
AW 13,15 is jumpered to module address $E4BE_H$

Binary input modules

The module addresses of all binary input modules (35 EB 90, 35 EB 91, 35 EB92) can be adjusted without interruption to this default jumpering of the PLC by means of their address switches.
The process image is registered automatically at the start of the program cycle.

Principle of functioning of the binary input modules: (Refer to the respective module description)

Binary output modules

The module addresses of all binary output modules (35 AB 90, 35 AB 94, 35 AB 95, 35 AB 96, 35 AB 97) can be adjusted without interruption to this default jumpering of the PLC by means of their address switches.
The process image is output automatically at the end of the program cycle. In multi-processor mode *several* PLC processors must *not* write to *the same* binary output group because the different PLCs will otherwise mutually overwrite each other's output values on the output device (see also the chapter entitled "Multi-processor operation"). Different programs *of one* PLC, however, may write to *one* binary output group. In this case, mutual overwriting is prevented by the PLC operating system.
The above statements also apply to super global values.

Principle of functioning of the binary output modules: Refer to the respective module description.

Analog input module of 35 EA 90 with 35 TP 90

Note:

The 35 EA 90 analog input module is **not** registered when creating the input image automatically. This module is served with the module of ANAEIN (see the block catalog).

The 35 EA 90 module is plugged onto the 35 TP 90 carrier board. 8 analog signals ranging from -10V...+10V or -5V...+5V can be connected. The 35 TP 90 carrier board can be used in any free address area within the input/output channels ($E000_H$...$FFFF_H$). On the MPST bus it occupies an address area of 256 bytes.

Principle of function of the analog input module: see the module description of 35 EA 90.

Analog input module of 35 EA 91 with 35 TP 90

The 35 EA 91 module is plugged onto the 35 TP 90 carrier board. 8 analog signals ranging from 4...20 mA can be connected. The 35 TP 90 carrier board can be used in any free address area within the input/output channels ($E000_H$...$FFFF_H$). On the MPST bus it occupies an address area of 256 bytes. The process image is registered **automatically** at the start of the program cycle (contrary to 35 EA 90). Addressing gaps occur.

However, it is possible to address the module by continuous EW operands by modifying the data block directory (DBV). For details of the principle of functioning of the analog input module: see the module description of 35 EA 91.