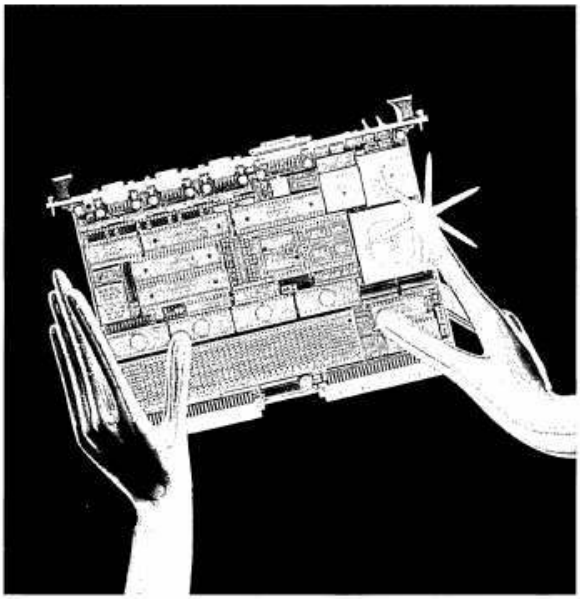


System 68000 VME

SYS68K/CPU-30

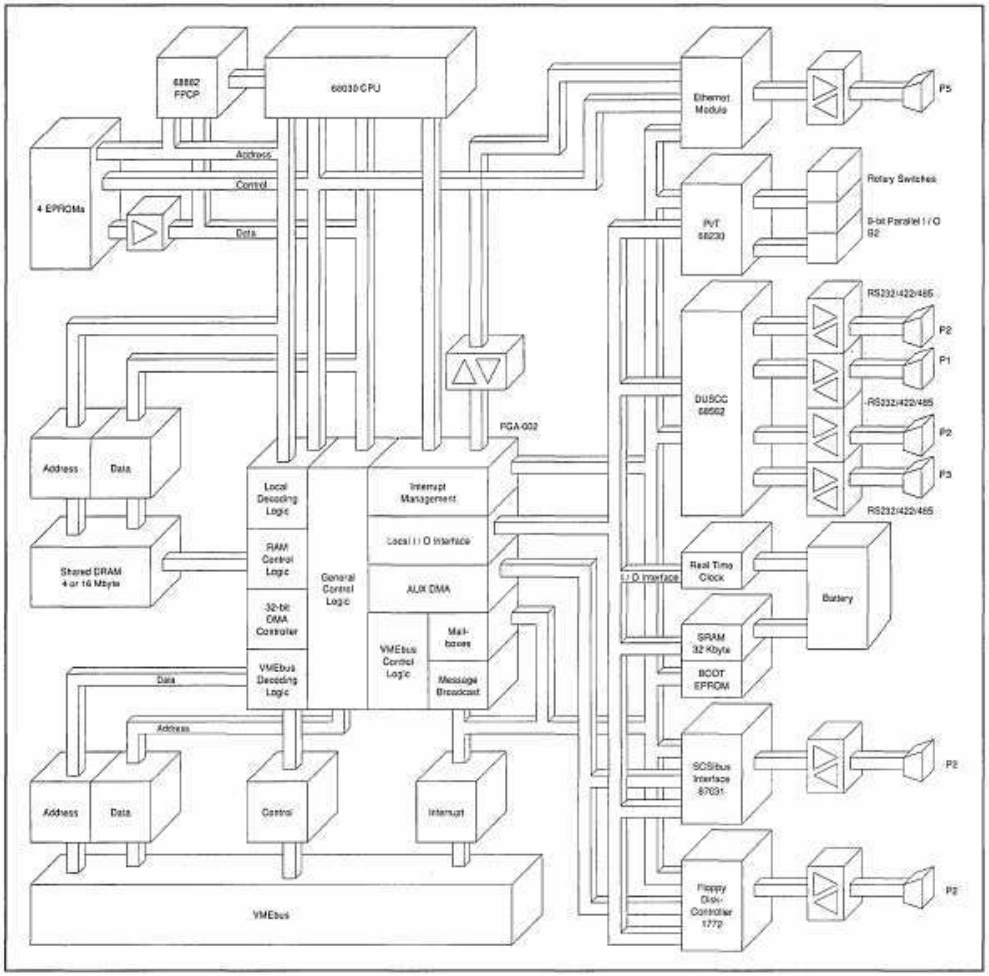
High Performance General Purpose 68030 CPU Board with Shared Memory, DMA and Mass Memory Control

General Description

The SYS68K/CPU-30 is a 68030/68882 based CPU board providing up to 16 Mbyte of shared memory. A full 32-bit DMA controller, supporting data transfers to/from VMEbus memory as well as to/from local RAM is provided by the 281-pin FORCE Gate Array (FGA-002).

Mass memory control is provided through a SCSI controller and a single chip floppy disk controller. Both are connected to the 32-bit DMA controller providing rapid data throughput to connected mass memory devices. Serial communication is provided through four fully independent multi-protocol channels. A LAN controller with its own 64 Kbyte data buffer allows the interconnection of the CPU-30 board via a standard Ethernet connector installed on the front panel. The LAN controller is available only on specific board versions. Additional features include up to 4 Mbyte EPROM capacity, 32 Kbyte SRAM and a Real Time Clock. VMEPROM, the Real Time Kernel, is installed by default. Two FORCE Message Broadcast channels and eight mailbox interrupts complete the board.

Block Diagram of the SYS68K/CPU-30



Features of the SYS68K/CPU-30

- 68030 CPU:
  20.0 MHz on CPU-30ZA
  25.0 MHz on CPU-30ZBE, -30BE/16
- 68882 FPCP:
  20.0 MHz on CPU-30ZA
  25.0 MHz on CPU-30ZBE, -30BE/16
- 32-bit high speed DMA controller for data transfers to/from the shared RAM and/or to/from VMEbus memory
  - 32-byte internal FIFO for burst DMA
- 4 or 16 Mbyte of shared DRAM with byte parity, supporting the 68030 burst fill mode
- The DRAM is accessible from the VMEbus via the FORCE Gate Array, FGA-002
- FORCE Message Broadcast (FMB)
- Four serial I/O interfaces, RS232/RS422/RS485-compatible
- 8-bit parallel interface with handshake
- Four system EPROM devices supporting 28- and 32-pin devices, using a 32-bit data path
  - 1 wait state access possible by using 100 nsec devices
- One boot EPROM for local booting and initialization of the I/O interface chips and the gate array
- 32 Kbyte SRAM with battery back-up on-board, using one 28/32-pin socket (JEDEC Standard)
- Real Time Clock with calendar and on-board battery back-up
- SCSI interface connected to the on-board DMA controller
- Floppy disk interface (SA460-compatible) for connection of 3", 3½" and 5¼" drives
- Local Area Network Controller for connection to Ethernet
- Two 24-bit timers with 5-bit prescaler
- One 8-bit timer
- All local I/O devices are able to interrupt the local CPU on a software-programmable level
- BERR handling fully under software control via different counters for local and VMEbus accesses
- Full 32-bit VMEbus master/slave interface supporting the following data transfer types:
  - A32, A24, A16 : D8, D16, D32 – Master
  - A32 : D8, D16, D32 – Slave
  - UAT and Read-Modify-Write cycles are also supported
- Single-level VMEbus arbiter
- SYSCLK driver
- VMEbus Interrupt Handler
- Support for ACFAIL* and SYSFAIL* via software-programmable IRQ levels
- Bus time-out counters for local and VMEbus accesses (15 µsec)
- VMEPROM, the Real Time Monitor with file manager and Real Time Kernel

1. Hardware Description

1.1 The 68030 CPU

The 68030 with its 32-bit address and data paths is installed on the SYS68K/CPU-30 board. The CPU includes a 256-byte instruction and a 256-byte data cache which significantly reduces the number of bus cycles needed for program fetches.
The 68030 CPU can access the DRAM in normal and burst fill mode. This allows the design to take full advantage of the throughput of the CPU.
Communication with the local I/O interfaces, local SRAM and the VMEbus interface to the 68030 CPU is provided through a specially designed 281-pin gate array, called FGA-002.
The EPROM area, the Floating Point Co-Processor and the shared DRAM are directly connected to the CPU data and address bus interface (as shown in the block diagram of the CPU-30).
The clock frequency of the 68030 CPU is 20.0 MHz or 25.0 MHz.

1.2 The Floating Point Co-Processor

The SYS68K/CPU-30 is fitted with the enhanced 68882 Floating Point Co-Processor (FPCP). The clock frequencies of the CPU and the FPCP are identical. The FPCP conforms to the IEEE 754 Floating Point Standard. Intercommunication between the CPU and the FPCP is built in silicon. An internal register set inside the FPCP of eight general purpose registers (80-bit wide) yields fast execution times.

Features of the FPCP

- Eight general purpose registers (80-bit : 64-bit mantissa, 15-bit exponent and 1 sign bit)
- 67-bit on-chip ALU
- 67-bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 Standard

Specifications

Function		
CPU/FPCP		68030/68882
CPU and FPCP clock frequency on:	CPU-30ZA CPU-30ZBE, -30BE/16	20.0 MHz
Shared DRAM capacity with parity	CPU-30ZA, -30ZBE CPU-30BE/16	4 Mbyte 16 Mbyte
SRAM capacity with on-board battery back-up		32 Kbyte
No. of system EPROM sockets Data path		4 32-bit
Serial I/O interfaces (68562) RS232/422/RS485-compatible		4 4
Ethernet interface on CPU-30ZAE and CPU-30ZBE Ethernet SRAM		AM7990 64 Kbyte
Parallel I/O interface (68230)		12 lines
Real Time Clock with on-board battery back-up		72421
SCSI interface (87031)		Single-ended
Floppy Disk Interface (WD1772)		SA 460
24-bit timer with 5-bit prescaler 8-bit timer		2 1
VMEbus interface Shared memory access time from VMEbus (read/write)	A32, A24, A16 : D8, D16, D32, UAT, RMW A32 : D8, D16, D32, RMW	Master Slave 900 nsec typ
SYSCLK driver Mailbox interrupts		yes 8
FORCE Message Broadcast	FMB-FIFO 0 FMB-FIFO 1	8 byte 1 byte
VMEbus and local interrupt handler All sources can be routed to a software-programmable IRQ level Total number of IRQ sources		1 to 7 yes 42
RESET, ABORT switches		yes
VMEPROM firmware installed on all board versions		yes
Power requirements	+ 5 V min : max + 12 V min : max – 12 V min : max	5.2 A : 6.0 A 0.1 A : 0.3 A 0.1 A : 0.3 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)		0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions		234 × 160 mm : 9.2 × 6.3 in
No. of slots used		1

Ordering Information

SYS68K/CPU-30ZA Part No. 101302	20.0 MHz 68030 based CPU board with 68882 FPCP, DMA, 4 Mbyte shared memory, 4 serial I/O channels, SCSI and floppy disk interface, VMEPROM. Documentation included.
SYS68K/CPU-30ZBE Part No. 101305	25.0 MHz 68030 based CPU board with 68882 FPCP, DMA, 4 Mbyte shared memory, 4 serial I/O channels, SCSI and floppy disk interface, Ethernet, VMEPROM. Documentation included.
SYS68K/CPU-30BE/16 Part No. 101306	25.0 MHz 68030 based CPU board with 68882 FPCP, DMA, 16 Mbyte shared memory, 4 serial I/O channels, SCSI and floppy disk interface, Ethernet, VMEPROM. Documentation included.
SYS68K/IOBP-1 Part No. 700043	Back panel for the CPU-30 boards providing serial I/O, SCSI and floppy disk controller connectors.
SYS68K/VMEPROM/30/UP Part No. 145109	VMEPROM update service for the CPU-30 series.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM user's manual, excluding the SYS68K/CPU-30 description.
SYS68K/CPU-30/UM Part No. 800146	User's manual for the SYS68K/CPU-30 including VMEPROM and FGA-002 user's manual.